AN IMPROVED NEW STRUCTURE OF SINGLE PARITY CHECK PRODUCT CODES

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Abstract: This paper proposes an improved new structure of Single Parity Check (SPC) product codes with an embedded interleaver. The complexity of decoding the new SPC product codes is the same as the one of the existing single parity check product codes by use of the message passing algorithm. Simulation results and bound analysis demonstrate a significant bit error rate (BER) performance improvement compared to the existing single parity check product codes for high code rates at medium signal-to-noise ratios (SNRs).

Key words: Product codes, single parity check codes, message passing algorithm.

1. INTRODUCTION

The single parity check (SPC) code is one of the most popular error detection codes because it is easy to implement. In these codes, the encoder adds one bit to a sequence of $n$ information bits such that the resultant $(n+1)$-bit codeword has an even number of ones. Two or more SPC codes can be used to construct a product code. These SPC product codes are referred to as SPC-I PC codes in this paper. SPC-I PC codes have been proven to exhibit an exceedingly good performance in terms of bit error probability [3]. The work in [1] and [2] studied the bit error rate performance under various decoding schemes. The work in [3] studied SPC multidimensional product codes in the additive white Gaussian channel. The work in [4] studied multiple serial and parallel concatenated single parity check codes, where simulation results showed that the four-stage serial or parallel concatenated SPC codes can outperform or perform as well as 16-state turbo codes, respectively. In this paper, we propose a new structure for SPC product codes with an embedded interleaver. The new structure of SPC is the same as two-stage parallel concatenated SPC in terms of code rate. The complexity of decoding the new SPC product codes is the same as that of the existing single parity check product codes by use of the message passing algorithm in [3], but the new SPC product codes have a significant BER performance improvement compared to the existing single parity check product codes at medium SNRs.

2. THE IMPROVED NEW STRUCTURE OF SPC PRODUCT CODES

The general structure of SPC-I PC codes is shown in Fig. 1. In Fig. 1, the encoder appends a single parity check bit to every row and every column. The lower right bit is a parity check bit on either row parity check bits or column parity check bits. SPC-I PC code rate is \( \left( \frac{n}{n+1} \right)^2 \). Every row and every column has an even number of ones after encoding. The decoder will perform iterative row-wise and column-wise decoding to recover the erased bits. When a single bit is erased in a row or column, it can be recovered by simple parity checking (mod-2 addition). If more than one bit is erased in a row or column, that row or column is skipped. Decoding will be performed until all erasures are recovered or the maximum number of iteration is reached.

Fig. 1 The structure of SPC-I product codes

Clearly, the SPC-I product code can recover all single, double, and triple erasure patterns. Patterns consisting of more than three erasures may or may not be recoverable. A pattern is unrecoverable if and only if it contains a sub-pattern such that every occupied row and every occupied column in that sub-pattern has at least two erasures. An unrecoverable error pattern is shown in Fig.2.

Fig. 2 An error pattern

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The unrecoverable error patterns are investigated in [6]. The reader may refer to [3] for more details.

The error pattern in Fig.2 may be recoverable if there is another parity check equation which contains any bit of the erasure pattern in Fig.2. If we use the SPC-I structure to get more parity check equations the penalty is that it lowers the system code rate. To keep the system code rate the same as SPC-I PC codes, one approach is to use more than n information bits in one parity check bit. For the message passing algorithm, it is preferable to have a parity check bit with a lower degree (fewer information bits) since in this case the information that it sends to its neighbors is more valuable. On the other hand, it is also preferable to have an information bit with a high degree (more information bits) since it will receive more information from the parity check bits, in this case allowing for more accurate judgment of the correct bit value. A number of researchers have examined the optimal degree distribution among bits [7]. The optimal distribution among bits, although interesting, will not be considered here. We propose to generate one parity check bit from two rows or two columns, i.e., one parity check bit for every 2n information bits. The new structure of SPC product codes, referred to as SPC-II PC codes is shown in Fig. 3. In Fig.3 the lower right bit is also a parity check bit on either row parity check bits or column parity check bits. For single SPC-II PC code the code rate is \( \left( \frac{n^2}{n^2 + n + 1} \right) \). Because of the structure of SPC-II PC codes n is limited to even number.

In order to compare SPC-II codes with the SPC-I PC codes studied in [3] in terms of code rates, two parallel concatenated SPC-II PC codes (2-PC-SPC-II PC) shown in Fig. 4 are employed in this paper. SPC-II PC encoder 1 generates n parity check bits on information bits and one parity check bit on parity check, while SPC-II PC encoder 2 generates n parity check bits on information bits because the parity check bit on parity check from SPC-II PC encoder 2 is the same the one from SPC-II PC encoder 1. The code rate of the 2-PC-SPC-II PC code is \( \left( \frac{n}{n+1} \right)^2 \). The decoding complexity of the 2-PC-SPC-II PC code is the same as that of the SPC-I PC code using the message passing algorithm in [3]. This is because the code rate of the 2-PC-SPC-II PC code is the same as that of the SPC-I PC code. Both 2-PC-SPC-II PC codes and SPC-I codes also have the same size of parity check matrix, \( H \).

3. PERFORMANCE BOUNDS AND APPROXIMATIONS

Firstly, we consider the SPC-I codes. The performance bounds and approximation of SPC-I codes discussed in [3] are summarized here below.

The union bound on the probability of bit error for a binary linear code over the AWGN channel is

\[
P_b \leq \frac{1}{2} \sum_{i=1}^{k} \frac{A_i}{k} \text{erfc} \left( \sqrt{R \frac{E_b}{N_0}} \right)
\]

where:
- \( k \) = the total length of information bits
- \( A_i \) = number of codewords of weight \( i \)
- \( R \) = code rate

Asymptotically, as the SNR tends to infinity, the term corresponding to the minimum distance of the code dominates the summation, leading to the following approximation:

\[
P_b = \frac{d_{\min} \cdot A_n}{2k} \text{erfc} \left( \sqrt{Rd_{\min} \frac{E_b}{N_0}} \right)
\]

where:
- \( d_{\min} \) is the minimum distance of the code.

Using the minimum distance and code rate and \( k = n^2 \), the resulting bound is
Secondly, we consider 2-PC-SPC-II PC codes. 2-PC-SPC-II PC codes are inherently a two dimensional parallel concatenated code. The union bound of the probability of bit error for parallel concatenated codes is given by \[ P_b \leq \sum_{w=0}^{2} \sum_{j=0}^{w-j} \frac{w}{k} A_{w,j} \cdot \text{erfc} \left( \sqrt{\frac{1}{2} \left( \frac{N}{E_b} \right) \left( \frac{w+j}{n+1} \right)} \right) \quad (4) \]

where:

\( k \) = the total length of information bits \\
\( N \) = the total length of the code \\
\( A_{w,j} \) is the number of codewords with input weight \( w \), parity weight \( j \), and the codeword weight is \( (w+j) \).

Asymptotically, as the SNR tends to infinity, the term corresponding to the minimum distance of the code dominates the summation. Here we only take into account \( w=2 \). The parity weight \( j \) of outputs has three possibility, 0, 2 and 4. In order to obtain an analytical expression for the union bound we merge parity weights 2 and 4 into 2.

Using \( k = n^2 \) and \( N = (n+1)^2 \) the union bound shown in Equ. (4) is approximated by

\[ P_b = \frac{9}{2(n^2-1)} \cdot \text{erfc} \left( \sqrt{\frac{1}{2} \left( \frac{N}{E_b} \right) \left( \frac{n^2-12}{n^2-1} \right)} \right) \quad (5) \]

4. SIMULATION RESULTS AND DISCUSSION

The performance of 2-PC-SPC-II PC codes is studied by simulation in the additive white Gaussian Channel. We assume perfect CSI and use BPSK. The system model for our simulation is based on Fig. 4. The message passing algorithm is employed at the receiver, with the number of iterations limited to 500. A random interleaver is employed. The codes simulated have rates 0.8789, 0.9431 and 0.9695 for both SPC-I PC and 2-PC-SPC-II PC codes, which are formed from \((16,17)^2\), \((32,33)^2\) and \((64,65)^2\), respectively. Fig. 5 to Fig. 7 show the bit error rate performance of these codes along with the corresponding union bounds, which are based on Equation (3) and (5), respectively. Fig. 8 shows the BER performance of 2-PC-SPC-II PC codes with different code rates. From Fig. 5 to Fig. 8, it can be seen that 2-PC-SPC-II PC codes demonstrate a significant performance improvement over SPC-I product codes. The coding gain tends to increase more as the signal-to-noise ratio increases from 4.5dB for both 0.8789 and 0.9431 code rates, and 5 dB for 0.9695 code rates, respectively. At BER of \( 10^{-5} \), a 0.25 dB gain is achieved for rate-0.8789 codes, while a gain at least 0.5dB is achieved for both rate-0.9431 and rate-0.9695 codes. The achieved gains show that 2-PC-SPC-II PC codes can recover most of the erasure patterns in Fig. 2. However, as the SNR increases the SPC-I code outperforms the 2-PC-SPC-II PC code. The thresholds are about 6.8dB, 7.8dB and 8.5dB, respectively. This is because SPC-II codes can achieve interleaving gains at medium SNRs. The 2-PC-SPC-II PC code can not achieve interleaving gain at high SNRs because low weight inputs dominate the BER performance. This also follows from union bound analysis.

5. CONCLUSION

In this paper we proposed a new structure of single parity check product codes, which have an embedded interleaver. We focus on 2-PC-SPC-II PC codes. The complexity of decoding the 2-PC-SPC-II PC codes is the same as the one for the existing single parity check product codes in terms of code rate, by use of the message passing algorithm. Simulation and bound analysis demonstrate a significant BER performance improvement over the existing single parity check product codes for high code rates at medium SNRs.

ACKNOWLEDGEMENT

The authors would like to thank the editor and anonymous reviewers for their valuable and constructive comments.
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Fig. 6 BER of SPC-I and 2-SPC-II PC code with R=0.94

Fig. 7 BER of SPC-I and SPC-II PC code with R=0.97

Fig. 8 BER of SPC-I and 2-SPC-II PC code with different code rates