A DESIGN OF A FREQUENCY HOPPING SPREAD SPECTRUM TRANSCEIVER FOR CDMA2000 SYSTEMS

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Abstract: This paper presents an integrated frequency hopped transceiver based on a subset of the cdma2000 network specifications. The circuit consists of a phase locked loop (PLL) that generates the hopping carriers, local oscillators (LOs) that generate GHz range carrier frequencies, and a series of mixers. It accepts input data in frequency shift keyed (FSK) format, and also outputs received data in FSK format.

Key words: CDMA, CMOS mixed signal circuits, FHSS, charge pump PLL, mixers, transceiver.

1. INTRODUCTION

Third generation (3G) cellular systems provide users with always-on connectivity, value added services (for instance, video conferencing), and networks that support truly global roaming. Achieving this requires more effective use of available radio spectrum, as well as considerably higher data rates than 2G systems. The method of choice for cellular networks to achieve the above is direct sequence spread spectrum (DSSS) technology. Systems using spread spectrum technology allow for greater security, noise/jamming rejection, and the use of code division multiple access (CDMA) methods for multiple user access.

Current commercial and academic integrated FHSS transceiver designs such as those described in [1] and [3] use the industrial, scientific and medicine (ISM) band to achieve high bit-rates (typically 160 kbps). The described design is implemented in the cdma2000 cellular band. This will make it compatible with existing cdma2000 1X environments. However, it will not be compatible with the network itself, due to differences in technologies used. FHSS is normally used in wireless LANs such as IEEE 802.11x.

The existing designs typically implement a proprietary RF subsection (amplifiers, filters, antennas). By not adding this RF section to the transceiver, this design allows different manufacturers to adapt the transceiver unit to customized RF specifications.

By not adding the FSK modulation on the transceiver, this unit also becomes semi-transparent to transmitted data. Any signal may now be transmitted, as long as it is encoded in FSK, and does not exceed the bit rate and bandwidth limitations of the transceiver. The reason for using FSK, is that frequency hops using PLLs are not phase-coherent, and hence a PSK system would involve significant overheads to implement.

2. DESIGN SPECIFICATIONS

2.1 General Specifications

The system must implement slow frequency hopping (equal to or lower than the bit rate) with a direct mixing architecture. Amplifiers and filters are to be implemented off-chip. The user must be able to manually select a hopping sequence, thereby identifying them on the network. The design is completed for the AMS 0.35 µm CMOS process, operating at 3.3V.

2.2 CDMA2000 Specifications

The CDMA2000 specifications mainly relate to frequency requirements for the system. Due to the complexity of a full cdma2000 system, and the fact that this system will not be compatible with the network itself (described in section 1), other specifications are relaxed somewhat. Motivation for usefulness of this design is given in the conclusion section. It is important to note that the transceiver will implement hopping within the channel as a means of CDMA (instead of DSSS), and not between different channels.

Only one forward and one reverse channel will be implemented with a bandwidth of 1.25 MHz each. The transmitter must operate at a base frequency of 1851.25 MHz, and the receiver at a base frequency of 1931.25 MHz. The system must support a bit rate of 120 bps (due to restrictions by the PLL architecture).

3. CONCEPT DESIGN

Figure 1 shows the concept design for the system. As described in the introductory paragraph, it does not include other RF components such as amplifiers, filters and antennas.
Hopping carriers are generated using a PLL, implemented using a charge pump architecture. The divider is implemented using an integer N configuration with a single divider in the feedback loop. The programmable divider is driven by a 4-stage pseudonoise (PN) generator, allowing a theoretical maximum of 15 users.

The generated hopping carriers are mixed up to GHz frequencies using single sideband (SSB) mixers. At the transmitter, the input data signal is then mixed up for transmission using a double sideband (DSB) mixer. The inverse procedure is performed at the receiver and the received wideband signal is mixed down to baseband.

Frequency planning is an important aspect of the system. The following table shows the various reference frequencies, frequency ranges and gains of the subsystems.

<table>
<thead>
<tr>
<th>Table 1: Frequency planning values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency point</td>
</tr>
<tr>
<td>-----------------</td>
</tr>
<tr>
<td>$f_{ref}$</td>
</tr>
<tr>
<td>Charge pump gain ($K_{PD}$)</td>
</tr>
<tr>
<td>Loop filter bandwidth</td>
</tr>
<tr>
<td>VCO sensitivity ($K_v$)</td>
</tr>
<tr>
<td>$\div N$</td>
</tr>
<tr>
<td>LO 1</td>
</tr>
<tr>
<td>Data (TX &amp; RX)</td>
</tr>
<tr>
<td>SS Signal (TX)</td>
</tr>
<tr>
<td>LO 2</td>
</tr>
<tr>
<td>SS Signal (RX)</td>
</tr>
</tbody>
</table>

4. MATHEMATICAL MODEL

To verify the concept, a mathematical model was first developed using MATLAB/Simulink. The model used standard Simulink blocks (such as PLLs and mixers), and Matlab code to control certain parameters in the model. The overall structure of the model closely resembles that of Figure 1.

Figure 2 shows the generated low frequency carriers.

5. SUBSYSTEMS

5.1 Phase Locked Loop (PLL)

Background: The ability to generate changing frequencies is fundamental to this FHSS system. Several documented methods exist, including direct analogue
synthesis (DAS), direct digital synthesis (DDS) and phase locked loops with frequency dividers.

This system uses a PLL operating at low frequencies from 150 kHz up to a maximum of 2.5 MHz. This reduces stringent design considerations inherent in high frequency PLL designs. The PLL method used is known as a charge pump PLL (CPPLL). It uses a phase frequency detector, a charge pump with integrated loop filter generating the control voltage, a voltage controlled ring oscillator and a programmable frequency divider in the feedback loop.

Due to the narrow bandwidth, low reference frequency and inherent speed limitations in PLLs, the system is limited in its achievable bit rate (120bps).

The sections below give descriptions of the various subsections of the PLL.

**Phase Frequency Detector (PFD):** The function of the PFD is to generate an error signal proportional to the difference in frequency (when there is a large difference between the output and reference signals), and phase (when there is a small difference between the output and reference signals), giving it an almost unlimited pull-in range. The PFD was implemented using D-type flip-flops and an AND gate. Figure 4 shows the basic structure. Note that these D-type flip-flops are customised, and do not have a standard input/output configuration.

The DC content of the QA (UP) and QB (DOWN) outputs contain information about the relative frequency and phase between the two inputs A and B [4]

The PFD does, unfortunately, suffer from some nonideal effects, affecting the performance of the CPPLL. This is explained as follows: If an ideal PFD that generates no pulses for zero input phase difference is used, for a very small phase difference, the pulse width at the QA or QB outputs will not be wide enough to allow it to rise to a logic level high enough to trigger the charge pump. Hence, for the abovementioned phase difference, the PFD cannot correct the error. This forms a dead zone, allowing a large amount of jitter to occur on the control voltage [4].

However, a PFD is not an ideal component, and reset pulses occur on the UP and DOWN lines, even with no phase difference present. These pulses are typically enough to allow the charge pump to deliver current eliminating the dead zone to a large extent.

**Charge pump and loop filter:** The UP and DOWN pulses generated by the PFD are used to charge and discharge the loop filter via the charge pump, generating the control voltage (CON) for the VCO. The structure of the charge pump and loop filter are shown in Figure 5.

M1 acts as a current source when turned on, charging the loop filter, and increasing the control voltage. M2 acts as a current sink when turned on, discharging the loop, and decreasing the control voltage. The transmission gate between QB and M2 acts as a delay element to minimize skew between QA and QB.

The loop filter is a 2nd order filter, with a loop bandwidth of 15 kHz. Due to the low operating frequencies, C1 becomes very large (several nanofarad), and therefore difficult to implement monolithically. The following equations are standard loop filter equations used in PLL design, adapted for this particular implementation. The parameters are as described in Table 1.

Equation (1) relates components values to natural frequency.

\[
\omega_n = \sqrt{\frac{K_f K_{PD}}{N C_1}}
\]  

(1)

Equation (2) relates component values to damping factor.
Equation (3) guides the selection of capacitor $C_2$ in the second order filter.

$$C_2 < \frac{C_1}{10}$$ (3)

**Voltage Controlled Oscillator (VCO):** The voltage controlled oscillator was implemented using a ring oscillator architecture, with differential delay cells. The differential layout allows the use of an even number of delay cells, with one pair cross-connected. This is necessary to generate the in-phase and quadrature-phase signals used to generate SSB signals in the mixers. Figure 6 shows a basic delay cell.

![Figure 6: Basic delay cell used in VCO](image)

The frequency of oscillation for a delay cell is given by Equation (4).

$$f_{osc} = \frac{1}{2NT_D}$$ (4)

The time delay $T_D$ is determined by resistance and capacitance seen at the output nodes of the cell.

As the oscillation frequency is controlled by changing the bias current using the bottom transistor, the amplitude of the output signal will change with the frequency. The addition of two additional transistors at the inputs alleviates this problem, with the output signal amplitude changing by only a factor of two over the frequency range of interest.

Since the frequency is controlled by current, a V-I converter is necessary between the loop filter and delay cells. The figure below shows the converter used, as well as the current mirrors necessary to replicate the current to all the delay cells.

![Figure 7: V-I converter with current mirrors](image)

At the output of the VCO, a custom hard limiting circuit (not shown), based on a differential amplifier and a modified CMOS inverter, generates the square wave necessary to drive to frequency divider, as well as the buffer divider between the VCO and the SSB mixers.

The output signal from the VCO to the mixers is divided by two due to design considerations, and hence the VCO operates up to 2.5 MHz, as opposed to the expected 1.25 MHz.

**Programmable Frequency Divider:** Frequency division involves comparing the value of a free running counter to some programmed value. Two types of counters were explored for use in the frequency divider design - reset counters and preset counters.

The former system starts counting up from 0 until it is reset when its value is equal to the programmed value. The latter starts counting from a programmed value and resets when it reaches the end of the counting sequence. By only counting over a limited range (as opposed to free running counters), these counters become modulo-$N$ dividers, where $N$ depends on the programmed value.

The counter that was implemented in this system is a preset counter, and is based on the 74x163 IC [8]. The core of the counter is a synchronous 4-bit counter, implemented using D type flip-flops.

The programmed start value is supplied by a connected PN generator, and the clock input is driven by the VCO. At the output of the divider, a T type flip-flop is used to generate the final output frequency. This is then compared to the reference frequency by the PFD.
As the divider produces an impractical result when the inputs are all high, the outputs of the PN generator are taken as inverted outputs. The PN generator never produces an all zeros output, hence the inverted outputs will never produce all high bits.

5.2 Pseudo-noise (PN) Generator

An m-stage shift register can be constructed by using several flip-flops. While flip-flops may be implemented using digital logic [8], it is uneconomical in terms of component count, speed and size. Instead, the flip-flop was implemented using a circuit element unique to CMOS circuits: the transmission gate [4].

By adding custom digital logic to the input of the D-type flip-flop, a programmable input with a control line was constructed. These programmable flip-flops are combined to form a programmable shift register. An XOR gate (modulo 2 adder) was connected to stages 1 and 4 of the circuit to form a programmable PN sequence generator.

The circuit is clocked at the desired hopping frequency (equal to or lower than the bit rate for a slow-hopping transceiver). The programmable inputs are controlled using low-level logic, uniquely identifying each user on the network.

5.3 Local Oscillators

Although they are easier to implement, ring oscillators are not suitable for high speed (> 1 GHz) operation, unless special circuit techniques are used such as in [6]. With on-chip passive inductors in CMOS processes being common, an LC tank oscillator is better suited to generate the GHz range carrier frequencies necessary for cdma2000 band operation.

The design used for this transceiver, is based on the design by [7], because of similar frequency ranges and process parameters. It uses an on-chip spiral inductor, with the initial and simulated values given in Table 2.

Table 2: Spiral inductor design parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Initial value</th>
<th>Final value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Outer diameter (µm)</td>
<td>300</td>
<td>289.6</td>
</tr>
<tr>
<td>Number of spirals</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Width (µm)</td>
<td>23.2</td>
<td>23.2</td>
</tr>
<tr>
<td>Pitch (µm)</td>
<td>18.1</td>
<td>18.1</td>
</tr>
<tr>
<td>Inductance (nH)</td>
<td>4.65233</td>
<td></td>
</tr>
<tr>
<td>Series resistance (Ω)</td>
<td>2.91</td>
<td></td>
</tr>
</tbody>
</table>

A single LC tank gain stage can be constructed by connecting the tank as the load to a transistor in feedback. By connecting two such stages in feedback, a cross-coupled differential oscillator is obtained. In [5], it has been shown that two such differential oscillators can be connected using additional NMOS transistors to produce quadrature waveforms. In such a cross-coupled oscillator, oscillations can only co-exist if they synchronise in quadrature. Figure 8 (at the end of the paper) shows the basic structure of such an oscillator, with bias current sources.

The inductor allows the oscillator to operate above the maximum supply voltage. To provide the correct common mode voltage between the oscillator and the next stage, the supply voltage is chosen as 2V.

The outputs are buffered through CMOS inverters (with minimal input capacitance), before being used as inputs to the mixers.

5.4 Mixers

Double Sideband (DSB) Mixer: The DSB mixers used were based on a passive commutating field effect transistor (FET) mixer design. They are used for up- and down-conversion of FSK data signals to and from cdma2000 carrier frequencies. The design is shown in Figure 9.

![Figure 9: Double sideband mixer](image)

Passive mixers have been compared to active mixers (such as the Gilbert cell) in [2]. Specifically, some of the advantages offered by passive mixers include simplicity, frequency stability, lower power consumption and high linearity.

The frequency limitation of the passive mixer depends essentially on the product of the off-capacitance and the on-resistance of the transistors used.

The inputs to the mixer are in-phase and 180° phase shifted signals LO outputs, and normal and inverted FSK signals.

Single Sideband (SSB) Mixer: SSB mixing uses the fact that summing or subtracting quadrature mixed signals will result in only a single sideband signal (upper or lower sideband), and hence no filters are necessary.
A SSB mixer is then constructed by connecting two DSB mixers as in the next figure, with each DSB mixer driven by either in-phase or quadrature-phase signals, as in Figure 10.

Figure 10: Single sideband mixer

5.5 Integration

The subsystems described were integrated to form a complete transceiver of the structure shown in Figure 1. The simulation results in the following section were obtained from the integrated subsystems.

6. RESULTS

6.1 PLL

The control output of the PLL when locking onto a frequency from rest is shown in Figure 11. It was generated from a SPICE simulation of the circuit.

Figure 11: PLL control output

The second order response is clearly visible, as well as the charge/discharge behaviour due to the charge pump.

The settling time, not taking into account the dead zone in the VCO, is measured, using additional plots, as approximately 0.09 ms for the maximum frequency jump of 2.3 MHz.

6.2 SSB Mixer

Figure 12 (end of paper) shows the FFT plot of the SSB mixer output, generated from a SPICE simulation of the circuit.

There is clear separation between the carrier of interest and other frequency components. There is some drift in carrier frequency because of the additional loading of the mixer on the oscillators.

6.3 DSB Mixer

Figure 13 (end of paper) shows the FFT plot of the DSB mixer output during upconversion, generated from a SPICE simulation of the circuit.

As depicted in Figure 13, clear separation between the data signals and the other frequency components is achieved.

7. CONCLUSION

This paper describes an integrated frequency hopped transceiver, based on a subset of the CDMA2000 specifications. It uses a charge pump PLL architecture to generate low frequency hopping carriers, and then a series of mixers to generate GHz range carriers, and translate FSK data signals up to and down from those carrier frequencies.

The transceiver operated as expected, on both mathematical and simulated circuit level. The calculated settling time of the PLL allows the transceiver to operate at the specified bit rate.

For optimal frequency stability in a cellular environment, the LC oscillators should be implemented in a separate PLL with a stable reference frequency. Mixer performance may also be improved by adding filters.

An issue that was outside the scope of the original problem, and hence not addressed, is synchronising between transceivers. This will typically be achieved by adding additional layers of signalling/information to the transmitted data, allowing low-level synchronising between transmitters and receivers.

For the reasons above (scope, implementation choices, desired additional features), the system was designed to be simulated as proof of concept. A hardware implementation should be viable with the abovementioned features included.
The project shows that it is indeed possible to implement FHSS technology in a DSSS dominated environment, using the frequency specifications for the DSSS system, at the cost of transmission speed. There are niche applications for such a system, such as in tracking beacons.

8. REFERENCES


