ISSN 1991-1696

Research Journal of the South African Institute of Electrical Engineers

Incorporating the SAIEE Transactions

SAIEE AFRICA RESEARCH JOURNAL Vol 101 No.1 pp 1-44

www.saiee.org.za

March 2010
Volume 101 No. 1

SAIEE AFRICA RESEARCH JOURNAL

(SAIEE FOUNDED JUNE 1909 INCORPORATED DECEMBER 1909)
AN OFFICIAL JOURNAL OF THE INSTITUTE
ISSN 1991-1696

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The following organizations have listed SAIEE Africa Research Journal for abstraction purposes:
INSPEC (The Institution of Electrical Engineers, London); "The Engineering Index" (Engineering Information Inc.)

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CBi electric
low voltage

GUEST EDITORIAL

SMEOS 2009 (SENSORS, MEMS AND ELECTRO-OPTIC SYSTEMS)

This special issue of the SAIEE Africa Research Journal is devoted to selected papers from the SMEOS 2009 (Sensors, MEMS and Electro-Optic Systems) Conference which was held in Skukuza, South Africa from 6 to 9 September 2009. The aim of SMEOS 2009 was to establish a forum for academia, research institutions and industry working in the field of sensors, MEMS and electro-optical systems, to share their relevant research and development ideas. Each paper presented at the conference was double-blind reviewed by at least two reviewers. Reviewers could recommend a reviewed paper to the technical chair for publication in this special issue, and a total of eight papers eventually passed this review process.

Four of the papers discuss the integration of additional functionality into existing CMOS processing. One paper addresses the issue of integrating MEMS devices onto a chip, and the other three investigate optical devices in the CMOS technology.

In the paper by Walton et al, *"Silicon^{+} - Post processing CMOS wafers to create integrated sensors, MEMS and electro-optic systems"*, the trend in recent years for many CMOS companies to diversify into new device types and associated novel application areas, is discussed. This paper examines many of the issues associated with integrating CMOS foundry and custom IC wafers with both new materials and technologies such as MEMS sensors and actuators.

The paper by Bogalecki and du Plessis, *"Design and manufacture of quantum-confined Si light sources"*, investigates the characteristics of quantum confined nanometre-scale SOI light sources in silicon technology. The realisation of effective light sources in silicon has been described as the "holy grail" of the silicon technology, and some advances towards this goal are described. The paper by Ellinghaus et al, "*A fully CMOS optical transmission system based on light emitting avalanche diodes*", illustrates the practical feasibility of a fully CMOS optical link, where an array of CMOS avalanche light emitting diodes is modulated with frequencies of up to 100MHz. Venter and du Plessis in their paper "*Feasibility of optical clock distribution for future CMOS technology nodes*" discuss the limitations on future CMOS scaling, which lie in the development of adequate interconnects to support the increase in logic density. This work aims to take the International Technology Roadmap for Semiconductors (ITRS) requirements for future technology nodes, to investigate the feasibility of optical clock networks as CMOS device dimensions decrease.

Two papers investigate optical detector materials. Odendaal et al in "*Surface passivation applicable to InAsSb/GaSb photodiodes for infrared detection*" investigate the influence of various anodisation solutions on the surface passivation of InAsSb/GaSb photodiodes for infrared detection, while Talla et al in "*ZnO grown by Metal Organic Chemical Vapor Deposition: Effect of substrate on optical and structural properties*", compare the influence of various substrates on the optical, structural and morphological properties of MOCVD deposited ZnO thin films in the UV and visible spectral range.

Two papers describe MEMS applications. In the first, "*Characterisation of adaptive fluidic silicone-membrane lenses*", Schneider et al present an alternative novel low cost adaptive fluidic silicone-membrane lens with an integrated piezo-actuator to alleviate the problem of laborious and costly exact mechanical positioning in autofocus systems based on the distance variation in lens systems. The paper "*3D ultra-fast manufactured micro coils on polymer or metal cores*" by Wallrabe et al presents high aspect ratio 3D solenoidal microcoils manufactured in a serial but ultra-fast and fully MEMS compatible winding procedure, using an automatic wirebonder. The applications of these coils include semi-integrated inductors for electronics, energy harvesting purposes, sensors and actuators.

Prof. Monuko du Plessis
Guest Editor

SILICON^{+} - POST PROCESSING CMOS WAFERS TO CREATE INTEGRATED SENSORS, MEMS AND ELECTRO-OPTIC SYSTEMS

A.J. Walton, J.T.M. Stevenson, I. Underwood, J.G. Terry, S. Smith, W. Parkes, C. Dunare, H. Lin, Y. Li, R. Henderson, D. Renshaw, B. Rae, K. Muir, M. Desmulliez[1], D. Flynn[1], M.J. MacIntosh[2], W.S. Holland[2], A. F. Murray, T.B. Tang and A. Bunting

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Abstract: Silicon based integrated circuit technology has shown astonishing progress scaling to smaller geometries as the industry follows Moore's predictions. However, in recent years the cost associated with staying at the leading edge of silicon IC technology has resulted in many companies being either unable, or unwilling, to afford the investment required. As a consequence some have decided to use foundry technology and/or diversify into new device types and associated novel application areas. All of these diverse Silicon^{+} technologies have one particular feature in common, namely they all use silicon as a platform for system integration with the added value being the innovation associated with post-processing and/or technology integration, which in many cases is realised on standard foundry technology. This paper examines many of the issues associated with integrating foundry and custom IC wafers with both new materials and technologies such as MEMS based sensors and actuators. In particular it examines the various options available for companies considering Silicon^{+} technology applications and presents examples of successful applications of this approach. Some of these are illustrated below.

Key words: silicon post processing CMOS integrated sensors, MEMS, electro-optic systems

1. INTRODUCTION

As the costs of following the International Technology Roadmap for Semiconductors (ITRS) [1] increase, a higher percentage of IC manufacturing companies are unable to afford the capital investment required to competitively manufacture the next technology node. To help reduce the risks most companies who are still committed to the next node in the roadmap, have joined forces with others to form consortia to reduce R&D costs by sharing the burden. Even with sharing the cost of developing technologies for the next generation of CMOS technology there is still a significant number of firms that are unable to sustain the investment required to follow Moore's law. These companies clearly have a technology resource they wish to exploit and are increasingly seeking to follow a more diversified business model to protect revenues. Hence, there is an interest in targeting products with additional functionalities deriving from biological, chemical, mechanical, optical, and other domains, to develop enhanced products and move into building systems rather than components. In following this strategy new and larger markets are created for these products, which have been traditionally outside the typical electronics-based portfolio of IC based companies. Some examples of these emerging technologies are detailed in the ITRS Roadmap and are listed below

- MEMS / Microsystems
- Photonics
- Plastics Electronics

The above technologies have one particular feature in common, namely they can they can be significantly enhanced by employing silicon as a platform for system integration. In this case the added value comes from the innovation associated with post-processing new/novel materials and technologies on CMOS or bipolar technology. In many cases this post-processing will be on standard foundry technologies taking full advantages of the economies of scale available as silicon microelectronics continues its remarkable evolution to smaller and smaller geometries.

Examples of this diversification that are presently being exploited includes smart power (integration of power devices with microelectronics), RF systems (integration of other semiconductor technologies such as SiGe, GaAs and passives with CMOS), microsystems (integration of a wide range of MEMS devices and sensors with CMOS), microdisplays (liquid crystal, light emitting polymers with the driving microelectronics on silicon directly underneath the display technology), bioelectronics (lab on a chip) and silicon photonics (integration of optical components on a silicon platform). All of these Silicon^{+}

technologies[*] have one element in common, namely the use of silicon as a platform for system integration with the added value being the innovation associated with post-processing and/or integration.

The attraction of silicon as a platform technology arises from its dominance as a high performance cost effective technology, which to date is unchallenged. However, it is clear that the scaling of Silicon IC technology cannot continue forever and either the economics associated with the reduction of dimensions or the limits of physics will initially slow and then halt the process. When scaling has run its course and the technology enters a more mature phase the importance of Silicon$^+$ as a source for innovation and new product developments will increase.
The vision of Silicon$^+$ in this paper is that it effectively treats the platform silicon integrated circuit (IC) technology as a commodity element of the system, and with much of mainstream CMOS being foundry based, the value added part becomes the bespoke processing and the associated IP. One of the attractions of this approach is that state-of-the-art CMOS technology is readily available without the need for any capital investment, which is a business model which has been very successfully exploited by so called fabless companies. The major appeal of this approach is that as foundry-processes are updated, the technology is immediately accessible making this element of any technology/product development future-proofed without the requirement for any significant capital investment. Hence, the potential exists for Silicon$^+$ based SMEs and startup companies to readily exploit new technology nodes as they become available.

This paper[•] will examine the options and challenges associated with integrating both foundry and custom IC technology with both new materials and other technologies such as MEMS (sensors and actuators) and present examples of the various options.

2. MEMS[‡]/CMOS[†] INTEGRATION

The performance of many sensors and Micro-Electro-Mechanical Systems (MEMS) can profit from being directly integrated with electronics. For example, there are great benefits in connecting pre-amplifiers and signal conditioning close to sensors, providing considerable advantages in performance and cost. Furthermore, if large arrays of sensors and/or actuators are required then backplane silicon electronics becomes essential.

There are a number of options available for integrating MEMS and CMOS integrated circuit technologies. The key requirements are to implement electrical, and in some cases thermal, interconnect between the CMOS and MEMS elements and some of the options that are available are listed below:

(a) The MEMS devices are fabricated on an electronic grade Silicon wafer and then encapsulated in oxide. The standard CMOS process then follows [2].
(b) Foundry wafers with the required electronics are fabricated and the MEMS is then post-processed on top [3, 4]
(c) A completely integrated CMOS and MEMS process is used [5].
(d) Manufacture of MEMS devices using etch release of structures built using material layers available and patterned as part of the CMOS process [21,22].
(e) MEMS and CMOS technologies (either in wafer or chip form) are individually fabricated and hybridised [6]
(f) Multi-chip modules
(g) Wafer bonding is used to integrate CMOS with MEMS [7,8]

The first four of these involve fabricating both the microelectronic devices and the MEMS technologies on a single wafer with the remaining ones involving integrating the technologies together after their separate fabrication. All of these approaches involve compromises and so have their individual attractions and limitations [3,4 ,8,9]. The following sections discuss the above approaches and their pros and cons.

2.1 MEMS processed on wafer before CMOS fabrication

In this format MEMS devices are fabricated in recesses in silicon wafers and effectively buried in oxide or some other suitable material [2] as shown in figure 1. The wafer is then planarised and the CMOS devices fabricated in the exposed silicon next to the device. The advantage of this approach is that the process is fully integrated, but the MEMS devices will experience all the high temperature steps associated with the CMOS process flow, which may cause problems for some structures. While this method of integration appears very attractive, a real practical issue with this technology is that contamination is a potential problem for all IC fabs, which precludes the use of many MEMS materials. Hence, if a MEMS fab is to manufacture the microsystem structures and bury them in oxide or some other material ready for the CMOS fabrication step then the IC foundry must have qualified the MEMS foundry to ensure that there are will be no possibility of contamination.

Another reason why this approach has not been widely adopted may be that the cost of processing the microelectronic circuitry (and also MEMS) is fixed

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[*] This approach is sometimes referred to as *More than Moore* (Scaling being More Moore) and/or *heterogeneous integration*
[•] This paper is based on a presentation give at an IET Symposium (2007) and an article in the NMI Year Book (2008).
[‡] In this paper MEMS is used in its widest sense to include all sensors and actuators.
[†] When CMOS integration with MEMS is referred to this should be considered to include other integrated circuit technologies such as bipolar, Bi-CMOS etc

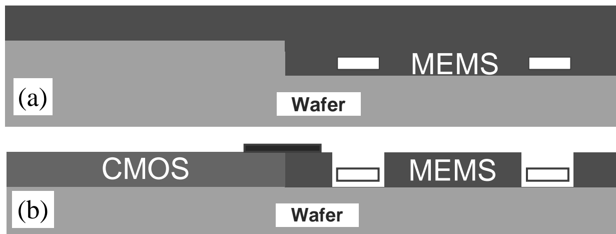

Figure 1. Schematic of MEMS processed on wafers before CMOS fabrication. (a) MEMS devices fabricated and buried in oxide which is then planarised to expose the silicon using CMP. (b) Finished process with metal interconnect between the CMOS and MEMS.

regardless of the number of devices on the wafer. Hence, the area occupied by the MEMS device can be considered to have a significant "microelectronics process" cost associated with it, especially if it is large. With the CMOS and MEMS wafer processing costs both effectively fixed, the end result is that MEMS processed on wafers before CMOS fabrication may provide significantly fewer systems than would be the case if the two technologies were fabricated on separate wafers and then assembled in a multi-chip module (see section 2.6) or as a chip on chip (see section 2.5). Obviously, where the benefits of direct integration outweigh the above considerations pre-processed MEMS will be viable but it is clear that there are significant cost penalties associated with using this approach when integrating the latest IC processes with large MEMS devices.

2.2 Foundry wafer post-processed with MEMS

Post-processing foundry CMOS involves procuring standard foundry processed wafers and then adding and patterning extra layers to create the MEMS device on top of the IC technology (see figure 2). The attraction of this approach is that the resulting system can select the most appropriate IC technology, and hence there is no problem procuring state-of-the-art technology should it be required. However, it should be remembered that mask sets for state-of-the-art IC technology are extremely expensive so post-processing integration with advanced processes is really only a feasible option for high volume products unless an existing design can be used as the IC backplane.

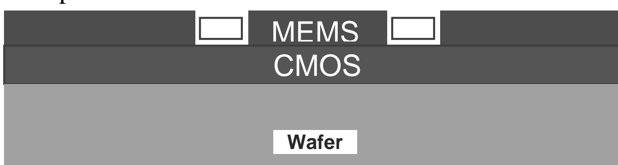

Figure 2. Schematic of foundry wafer post-processed with MEMS.

Post-processing has many attractions but one of its limitations is that the maximum processing temperature is limited to not more than 450°C to protect the integrity of the CMOS, making the use of materials such as polysilicon for resonators during the post-processing phase impractical. Possible replacements that have been proposed are germanium and SiGe [10,11] that can be deposited at 400-450°C.

There are many other standard IC (and non-standard) materials which can be deposited and patterned. Examples of companies whose commercial products follow this approach are MicroPix, (now 4D - Liquid Crystal alignment and spacer technology for LC microdisplays [12]) and Vision (before being acquired by ST Microelectronics – CMOS imagers with micromachined lenses and colour filters [13]). Another company that has successfully used this approach of post-processing foundry CMOS is Microemissive Displays (MED) with their organic light emitting diode (OLED) microdisplays [14]. Other technologies suited to this implementation include the fabrication of detectors [15] and ElectroWetting On Dielectric (EWOD) [16] devices on silicon IC backplanes. Figure 3 (a) shows an example of an EWOD chip with 25 electrodes for moving liquid droplets while figure 3 (b) shows EWOD electrodes (with a 100μm pitch) integrated with SPADs (Single Photon Avalanche Diodes). Many of the above commercialised application specific technologies that were originally post-processed have matured to the stage where they have now become part of a foundry's standard offering. Finally, it should be remembered that the post-processing option enables the final fabrication steps to be either undertaken in a custom built process line or in a contract run MEMS facility, which provides opportunities for second sourcing.

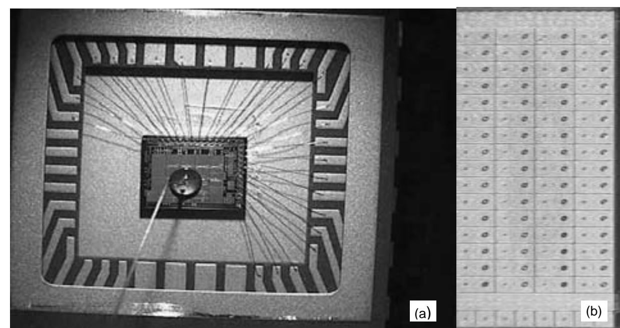

Figure 3. (a) A 25 electrode CMOS EWOD chip. (b) EWOD chip with integrated SPADs on each electrode.

2.3 Total integration of MEMS and CMOS processes

This option requires access to an integrated fabrication facility and is really only open to companies and organisations that are more vertically integrated having both CMOS and MEMS technology available (figure 4). The drawback of this approach is that, if there is a need to

Figure 4. Schematic of the total integration of MEMS and CMOS processes.

future proof a business by keeping in-house IC technology following the roadmap, then extremely high levels of investments are required. Two examples of companies in a position to take the full integration approach, but who perhaps have not been fully committed to following the roadmap, are Texas Instruments and Analog Devices. Both have significant shares of the MEMS market with TI fabricating their Digital Micro Mirror (DMM) display system† [17] and Analog Devices their accelerometer and gyro products [18,19]. The commercial barriers to entering the market using this approach are significant as it requires a fabrication facility with both CMOS and MEMS capability, which even if the CMOS technology is not state-of-the-art, still requires significant investment. However, it does enable both the MEMS and CMOS to be optimised within the constraints of the process flow employed.

2.4 CMOS process with MEMS etch release/access post-process

In this approach, the CMOS wafer is fabricated in the standard manner with the design already incorporating the layout required by the MEMS device [20]. At the completion of the CMOS process all that is required is a simple etch release step as shown schematically in figure 5. Examples of this include diffraction gratings / light filters using the multilevel fine metal pitch available with the latest processes [21], releasing mechanical structures such as comb-drive resonators, cantilever beam arrays and accelerometers [22,23], copper structures [24] and pH sensors for a pill that is swallowed (figure 6) [25,26]. Reference [3] also gives more examples of the above approach for a number of different technologies.

This method of CMOS foundry technology with MEMS etch release can obviously be used in combination with post-processing extra patterned layers either before or after the etch release step. As with standard post-processing the above approach can take full advantage of the latest IC technology with sub-micron polysilicon and metal structures being available and of course copper and low κ materials.

Figure 5. Schematic of a CMOS process with MEMS etch release/access post-process.

2.5 Hybridisation

This scheme involves taking separately processed CMOS and MEMS wafers (or chips) and then hybridising or

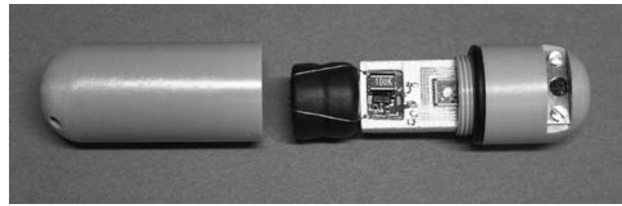

Figure 6. Sensors in a pill [25] suitable for CMOS / MEMS sensor fabricated by post CMOS etching [26].

bump bonding them. This is a standard process that is widely used for IC packaging/interconnect and providing processing temperatures < 450°C (the maximum temperature for CMOS ICs) are used hybridisation is very straightforward (see figure 7).

However, for some MEMS devices the materials and or structures will not survive temperatures approaching this maximum. If low temperature bumping is required then there are a number of options that include indium [27] and gold ball bumping [28]. An example utilising indium bumps is the SCUBA-2 sub-millimetre bolometer detector [6] shown in figure 8. This 4×5cm device has 218,000 indium bump bonds providing both thermal and electrical connection between the upper pixel array and the underlying SQUID multiplex device. An example using gold bumping is the creation of micro-inductors [28], images of which are shown in figure 9. Alternatively, eutectic die bonding of CMOS - MEMS technology has been demonstrated by Austria Microsystems to produce a polysilicon based capacitive acceleration sensor bonded onto a CMOS chip containing the sensing electrode and read-out electronics [29].

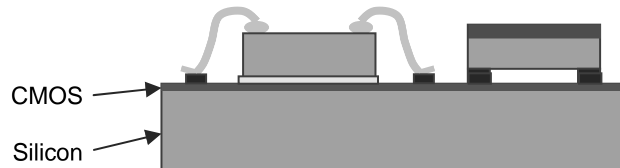

Figure 7. Flip chip and wire bonding hybridisation.

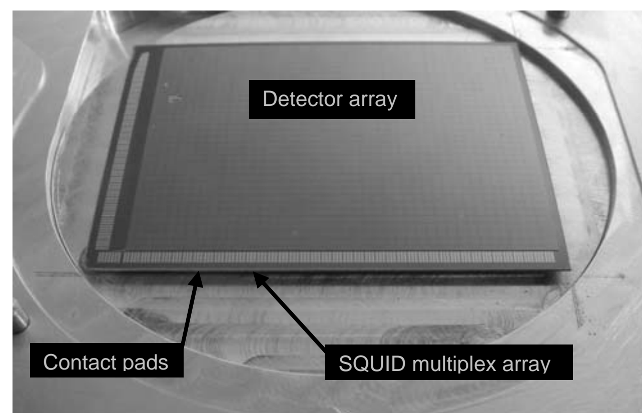

Figure 8. One quadrant of the detector array for SCUBA-2. The detector is hybridised to the bottom chip with 218,000 indium bump bonds to provide both electrical and thermal conduction.

† Note that while the DMM technology comes from a company that manufactures ICs and can be considered fully integrated the MEMS process is built on top of the electronics and so could be considered as post-processed.

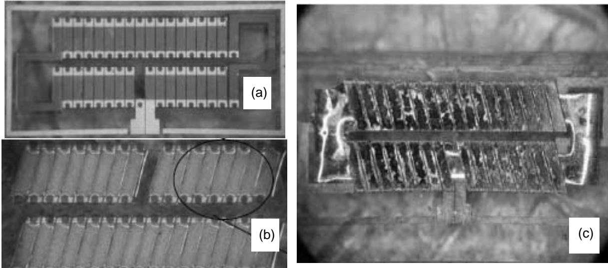

Figure 9. Fabricated micro-inductor (a) bottom, (b) top of an inductor before bump bonding, (c) micro-inductor of size 2mm×5mm×250μm (W×L×T). The nickel windings are clearly visible diagonally. The Ni(80)Fe(20) core of ring is assembled between the windings by flip-chip bonding.

It is possible to attach the MEMS device to the CMOS wafer (or *vice versa*) and subsequently provide the interconnect between chips with wire bonding (chip on chip). A further hybrid-type approach is to use what could be considered a non-MEMS technology hybridised with a CMOS backplane [30], a method used in proof of concept devices for the post-processed detector technology reported in reference [15].

2.6 Multi-chip Modules

Using multi-chip modules is a standard approach for assembling more than two ICs and other components, e.g. chip capacitors, into an electronic module. Being such a readily available technology this has a low entry barrier and can be used for many applications. A large number of manufacturers, including Bosch, Motorola (Freescale) and SensoNor use this approach with many of their MEMS based systems.

2.7 Wafer bonding of CMOS and MEMS wafers

Fabricating MEMS and CMOS devices on separate wafers enables the optimisation of each technology independently. Hence, there are many potential attractions if the two wafers can be combined together. However, bonding two wafers together, to integrate the two technologies, requires a low temperature (<450°C[†]) bonding step to prevent any thermal effects or damage to the processed wafers. In addition, some method of electrically connecting the bonded wafer pair and bringing the electrical signals to the top surface also needs to be implemented. The electrical interconnect issue has many solutions that are well documented in 3-D interconnect research such as [31,32]. References [7,8] present details of test structures that have been designed to examine the feasibility of integrating prefabricated MEMS and CMOS devices (see figure 10), using chemical mechanical polishing (CMP) and low temperature wafer bonding. An example of this is shown in figure 11.

[†] Note: This temperature can be considerably lower depending upon the materials being used

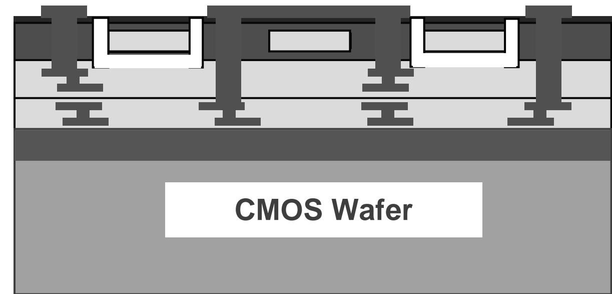

Figure 10. Schematic of integrating MEMS with CMOS using wafer bonding and thinning.

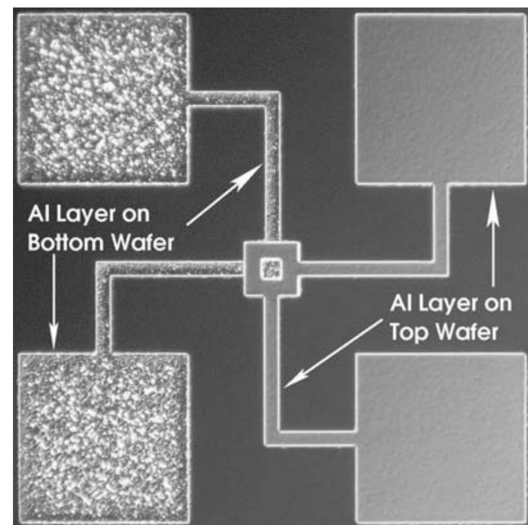

Figure 11. Bonded and electrically connected structures (via in centre of photograph). The top silicon handle wafer has been removed and the pattern on the bottom wafer can be viewed through the oxide.

Wafer bonding requires that the CMOS and MEMS die must be designed to have the same pitch on the wafer which can lead to unused areas of silicon on one of the wafers. From a commercial point of view the best ratio for the CMOS and MEMS working areas is 1:1 where there is no unused/wasted real estate for either the CMOS or MEMS technology. Figure 12 shows this effect as a

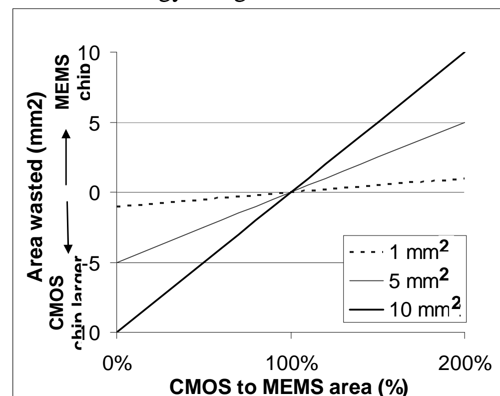

Figure 12. Relationship between MEMS and CMOS area that remains unused for bonded wafers as the ratio of the chip size of the two technologies varies. MEMS and CMOS chip sizes are 1, 2 and 10mm^2 when CMOS to MEMS chip area ratio = 100%.

function of chip size and ratio of CMOS to MEMS chip area. Obviously with chip based hybridisation there is not such an issue as the chips are diced before interconnect and hence there is no need for the chips to be identical sizes.

3. DISCUSSION AND CONCLUSIONS

The exponential increase in IC performance, which has followed Moore's Law for 40 years, has used the ITRS (International Technology Roadmap for Semiconductors) scaling rules to good effect. This has enabling the IC industry and its customers to plan their businesses effectively, as the roadmap has reliably predicted the rollout and price/performance of the next generation circuit node. With the maturing of silicon IC technology, following the roadmap has become more expensive and the number of active players has reduced. Further shrinking of the component scale is now approaching physical and economic limits, while at the same time microelectronic devices are becoming all pervasive within society and are increasingly being combined with a plethora of other sensing and processing technologies. We face a disruptive discontinuity in that:

- A large percentage of IC companies will not be able to afford to continue following the ITRS roadmap (this has already happened to almost all the UK based manufacturing operations) and the industry will increasingly have to follow a diversified business model to protect revenues.
- Beyond traditional IC electronic processing, the incorporation of additional functionalities deriving from biological, chemical, mechanical, optical or other domains will increasingly be targeted by IC companies to develop enhanced silicon technology, creating new and larger markets beyond the existing electronics-based openings.

This presents CMOS and MEMS technology with new methods of enabling continued growth in the performance of IC technology through the innovative implementation and integration of MEMS, novel materials and technology with silicon ICs.

Exploiting the technological opportunities at the interface between silicon electronics, engineering and the physical and life sciences is obviously crucial to the objective of following the opportunities presented by Silicon$^+$. Developments in this area will, for example, see a transformation in devices such as bioarrays, sensors and medical diagnostics, which integrate state of the art semiconductor technology with surface chemistry and biochemistry and which necessitate interdisciplinary collaboration. In parallel, there is the potential to harness existing technologies and integrate them with new materials and other circuitry. Therefore, with appropriately multi-skilled teams it will be possible to harness the power of photonics, microfluidics, chemical sensing and micro-mechanical functions with the processing power of electronics. This in turn will help create new and exciting opportunities for both research and industry centred on the effective implementation of MEMS related technology using silicon as a high-performance versatile platform technology.

Process	Cost barrier to entry	Wafer scale	Pre-tested dies	Commercial availability	Die assembly	High temp MEMS
Pre-CMOS MEMS Integrated	Medium/ High	Yes	No	Limited	No	Yes
Post-processed MEMS on CMOS	Medium	Yes	No	Some processes	No	No
Integrated CMOS and MEMS	High	Yes	No	Extremely limited	No	Possible
CMOS and MEMS with etch release	Medium/Low	Yes	No	Yes	No	Possible
Hybridisation	Low	Yes	Yes - die/die No - waferscale	Yes (die)	Yes	Yes
Chip on chip	Low	No	Yes	Yes	Yes	Yes
Multi-chip Module	Low	No	Yes	Yes	Yes	Yes
CMOS/MEMS wafer bonding	Medium	Yes	No	No	No	Yes

Table 1. Comparison of different CMOS / MEMS integration technologies.

The method of integration selected will be entirely driven by cost and table 1 compares some aspects of the different options. One issue for all the options is the availability of second sourcing which is usually required and this may be more problematic for the fully integrated approach, although large vertically integrated companies usually have more than one manufacturing site.

The post-processing option has many attractions to start-up companies as has been illustrated by companies such as MED, MicroPix and Vision (ST), who have successfully developed microdisplays and CMOS imagers. While it is clear that some options are only available to large IC companies, the post-processing option can clearly be successfully exploited by a wider range of organisations as can the hybridisation related approaches. Both of these approaches have a lower cost of entry and so have attractions.

4. REFERENCES

1. ITRS Roadmap available from http://www.itrs.net/
2 J. H. Smith, S. Montague, J. J. Sniegowski, J. R. Murray, P. J. McWhorter, "Embedded Micromechanical Devices for the Monolithic Integration of MEMS with CMOS", IEDM Technical Digest, pp. 609-612, 1995.
3 H. Baltes, O. Brand, A. Hierlemann, D. Lange, C. Hagleitner, "CMOS MEMS - Present and Future", Technical Digest, Fifteenth IEEE International Conference on Micro Electro Mechanical Systems, pp. 459-466, 2002.
4 J. Schmitz, "Adding functionality to microchips by wafer post-processing", Nuclear Instruments and Methods in Physics Research A, Volume 576, no 1, 11 June 2007, pp 142-149
5 T. Scheiter, H. Kapels, K.-G. Oppermann, M. Steger, C. Hierold, W.M. Werner and H.-J. Timme, "Full integration of a pressure-sensor system into a standard BiCMOS process", Sensors and Actuators A: Physical, Vol. 67, Issues 1-3, pp. 211-214, May 1998
6 W. Parkes, C.C. Dunare, A.J. Walton, J.G. Terry, J.T.M. Stevenson, A.S. Bunting, A.M. Gundlach, S. Smith, G.C. Hilton, K.D. Irwin, J.N. Ullom, W.D. Duncan, W.S. Holland, M.D. Audley, M.J. MacIntosh, M. Ellis, P.A.R. Ade, R. Sudiwala and E. Schulte, "Design and fabrication of the SCUBA-2 detector for the JCM telescope", IEE Seminar on MEMS Sensor Technologies, London, 25 April 2005, 8/1-8/5
7 H. Lin, A.J. Walton, C.C. Dunare, J.T.M. Stevenson, A.M. Gundlach, S. Smith, A.S. Bunting; "Test Structures for the Characterisation of MEMS and CMOS Integration Technology", IEEE International Conference on Microelectronic Test Structures, pp. 143-148, 6-9th March 2006.
8 H. Lin, J.T.M. Stevenson, A.M. Gundlach, C.C. Dunare, A.J. Walton, "Application of CMP for Integrating MEMS and CMOS Technology", 16th European Workshop on MicroMechanics (MME), pp. 207-210, 2005.
9 O. Brand, "Microsensor Integration into Systems-on-Chip", Proceedings of the IEEE, 94, no. 6, pp. 1160-1176, 2006.
10 A.E. Franke, D. Bilic, D.T.Chang, P.T. Jones, T.-J. King, R.T. Howe, G.C. Johnson, "Post-CMOS integration of germanium microstructures", Twelfth IEEE International Conference on Micro Electro Mechanical Systems, 1999. MEMS '99, Orlando, FL, USA. pp 630-637, Jan 1999
11 A. Kovalgin, J, Holleman, "Low-Temperature LPCVD of Polycrystalline GexSi1−x Films with High Germanium Content", Journal of The Electrochemical Society, vol 153, pp G363-G371, 2006
12 A.J. Walton, D.G. Vass, I. Underwood, G. Bodammer, D.W. Calton, K. Seunarine, J.T.M. Stevenson, A.M. Gundlach; "A Review of the History and Technology of Micromachined Miniature Displays Using Foundry Produced Silicon Backplanes", SPIE Design, Characterisation, and Packaging for MEMS and Microelectronics, 3893, pp. 26-38, 27-29th October 1999.
13 C. Fossati1, O. Gagliano1, M. Commandre1, B. Dunne, "Microlens design for CMOS image sensor", Proc. SPIE vol. 5962, Optical Design and Engineering II pp. 696-703, 2005.
14 I. Underwood, J. Gourlay, "Light-emitting polymer on CMOS: a new photonic technology?", Wave Optics and Photonic Devices for Optical Information Processing II. Edited by Ambs, Pierre; Beyette, Fred R., Jr. Proceedings of the SPIE, Volume 5181, pp. 110-119, 2003
15 V. M. Blanco Carballo, M. Chefdeville, H. van der Graaf, C. Salm, A. A. I. Aarnink, S. M. Smits, D. M. Altpeter, J. Timmermans, J. L. Visschers, J. Schmitz, "A miniaturized multiwire proportional chamber using CMOS wafer scale post-processing", ESSDERC, pp 129-132, 2006
16 Y. Li, P. Li, A Kazantzis, L.I. Haworth, A W S Ross, J G Terry, J T M Stevenson, A M Gundlach, A. Bunting, A.J. Walton; "Building EWOD microfluidic array technology on top of foundry CMOS", IET Seminar on MEMS Sensors and Actuators, pp. 25-30, 27-28 April 2006.
17. F. van Kessel, L.J. Hombeck, R.E. Meier, M.R. Douglass, "A MEMS-based projection display", Proc. IEEE 86, no 8, Aug, 1998, pp 1687-1704.
18 S. Lewis, S. Alie, T. Brosnihan, C. Core, T. Core, R. Howe, J. Geen, D. Hollocher, M. Judy, J. Memishian, K. Nunan, R. Paine, S. Sherman, B. Tsang, B. Wachtmann, "Integrated Sensor and Electronics Processing for >10^8 IMEMS Inertial Measurement Unit Components", IEDM, pp 39.1.1-39.1.4, 2003
19 B. Scannell, "Integrated MEMS Sensors for Industrial Control", EPN, Jan 2007
20 D.F. Guillou, S. Santhanam, L. R. Carley, "Laminated, Sacrificial-poly MEMS Technology in Standard CMOS", Sensors and Actuators A (Physical), 85, pp. 346-355, 2000.
21 C-L. Dai, H-L. Chen, C-Y. Lee, P.-Z. Chang, "Fabrication of diffractive optical elements using the CMOS process", J. Micromech. Microeng. Vol 12 pp 21–25, 2002
22 X. Huikai Xie, L. Erdmann, Z. Xu, K, Gabriel, G.K. Fedder, "Post-CMOS processing for high-aspect-ratio integrated silicon microstructures", Journal of Microelectromechanical Systems, Vol 11, No 2, pp 93-101, April 2002
23 H. Luo, G. Zhang, L.R. Carley, G.K. Fedder, "Post-CMOS Micromachined Lateral Accelerometer", Journal MicroElectromechanical Systems, pp188-195, Vol. 11, No. 3, June 2002
24 X. Zhu, S. Santhanpn, H. Lakdawala, H. Luo, G.K. Fedder., "Copper interconnect low-k dielectric post-

CMOS Micromachining", Transducers 2001 Digest of Technical Papers, pp. 1548-1551, 2001.

25 T.B. Tang, E.A. Johannessen, L. Wang, A. Astaras, M. Ahmadian, A.F. Murray, J.M. Cooper, S.P. Beaumont, B.W. Flynn, D.R.S. Cumming; "Toward A Miniature Wireless Integrated Multisensor Microsystem for Industrial and Biomedical Applications", IEEE Sensors Journal: Special Issue on Integrated Multisensor Systems and Signal Processing, 2, 6, 628-635, 2002

26 P.A. Hammond, D.R.S. Cumming, D. Ali, "A single-chip pH sensor fabricated by a conventional CMOS process", Proceedings of IEEE Sensors. Vol 1, pp 350- 355, 2002

27 A.J. Walton, W. Parkes, J.G. Terry, C.C. Dunare, J.T.M. Stevenson, A.M. Gundlach, S. Smith, G.C. Hilton, K.D. Irwin, J.N. Ullom, W.D. Duncan, W.S. Holland, M.D. Audley, H. McGregor, P.A.R. Ade, R.V. Sudiwala, A.L. Woodcraft, E. Schulte; "Prototype Detector Technology for the SCUBA-2 Sub-millimetre Bolometer Array", Journal of Nanoengineering and Nanosystems: Proc IMecE Part N, 219, pp. 11-21, 2005.

28 D Flynn, R S Dhariwal and M P Y Desmulliez, "A design study of microscale magnetic components for operation in the MHz frequency range", J. Micromech. Microeng. Vol 16, 2006, pp 1811–1818

29 M. Brandl, V. Kempe, "High performance accelerometer based on CMOS technologies with low cost add-ons", Proc .IEEE MEMS 2001, pp. 6-9, 2001

30 M. Campbell, M. Chefdeville, P. Colas, A.P. Colijn, A. Fornaini, Y. Giomataris, H. van der Graaf, E.H.M. Heijne, P. Kluit, X. Llopart, J. Schmitz, J. Timmermans, J.L. Visschers, "Detection of single electrons by means of a Micromegas coveredMediPix2 pixel CMOS readout circuit", Nuclear Instruments and Methods in Physics Research A, vol 540pp 295–304, 2005

31 J-Q Lu, Y. Kwon, G. Rajagopalan, M. Gupta, J. McMahon, K-W. Lee, R.P. Kraft, J.F. McDonald, T.S. Cale, R.J. Gutmann, B. Xu, E. Eisenbraun, J. Castracane, A. Kaloyeros, "A wafer-scale 3D IC technology platform using dielectric bonding glues and copper damascene patterned inter-wafer interconnect", Proceedings of the IEEE 2002 International Interconnect Technology Conference, pp 78- 80, 2002.

32 N. Ranganathan, N. Jiang, E. Liao, C.S. Premachandran, K. Prasad, N. Balasubramanian, "Through-wafer interconnection by deep damascene process for MEMS and 3D wafer level packaging", Proceedings of 7th Electronic Packaging Technology Conference, 2005. EPTC 2005, 5pp, 7-9 Dec. 2005

DESIGN AND MANUFACTURE OF QUANTUM-CONFINED SI LIGHT SOURCES

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Abstract: To investigate quantum confinement effects on silicon (Si) light source electroluminescence (EL), nanometre-scale Si finger junctions were manufactured in a fully customized silicon-on-insulator (SOI) production technology. The wafers were manufactured in the cleanroom using an electron-beam pattern generator (EPG). The SOI light source with the highest irradiance emitted about 9 times more optical power around λ = 850 nm than a 0.35 µm bulk-CMOS avalanche light-source operating at the same current. It is shown that the buried oxide (BOX) layer in a SOI process could be used to reflect about 25 % of otherwise lost downward-radiated light back up to increase the external power efficiency of SOI light sources.

Key words: Nanometre-scale SOI, Silicon light source, Quantum confinement, Silicon electroluminescence.

1. INTRODUCTION

1.1. Problem statement

While on-chip silicon (Si) optical transmission, detection and manipulation elements are already practically achievable [1], a suitably efficient on-chip Si light source is not yet available. Although light emission from Si was observed as early as 1955 [1] and its high-speed capability [2] and long-term reliability [3] are established, the major reason for the inherently weak light emission of Si is its indirect band-gap [5]. While alternative light-sources have been proposed [1], most require special manufacturing steps that are not easily implemented in the currently prevailing CMOS manufacturing technology.

The authors have been developing Si light sources since 1992 [5]. Si (electroluminescence) EL improvement research within the INSiAVA[1] project has focussed on promising light source configurations that include *inter alia* avalanche, punch-through and carrier-injection [6] Si light sources.

1.2. Quantum confinement

EL enhancement factors of up to 30, due to quantum-mechanical confinement in ultra-thin Si compared to bulk devices, have been reported ([7] - [10]). References [7] and [8] reported a strong efficiency improvement in forward-biased SOI LEDs on a buried oxide (BOX) when the thickness of the regions shown in Figure 1 was reduced. The dramatic increase in integrated EL with reduced device layer thickness (Figure 2) was attributed to the suppression of non-radiative recombination.

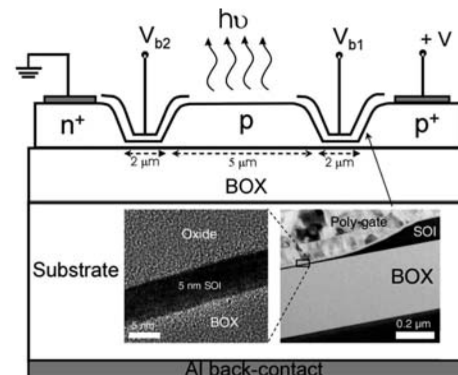

Figure 1: SOI LED manufactured in [7] and [8].

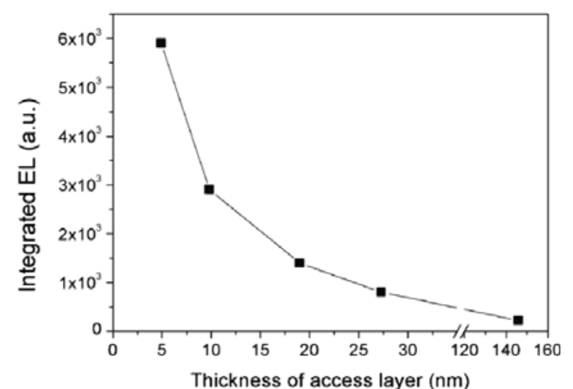

Figure 2: EL intensity against access layer thickness [8].

The abovementioned SOI light sources are only thin in one dimension (1D), their planar thickness, with device

[1] The Carl and Emily Fuchs Institute for Microelectronics (CEFIM) at the University of Pretoria (UP) in South Africa researches Si EL improvement with financial support from INSiAVA (Pty) Ltd.

widths ranging between 20 and 60 µm. It should also be noted that their *pn*-junctions are located outside the thinned area.

1.3. Objective

The main purpose of this work was to design and manufacture SOI light sources that would enable the investigation of quantum confinement effects on EL characteristics like external power efficiency and spectral emission in avalanche, punch-through and carrier-injection Si light sources. Instead of just creating planar thin 1D quantum-confined SOI light sources, the technical objective was to design and manufacture devices that are smaller in two dimensions, i.e. two-dimensional (2D) quantum-confined SOI light sources. With reference to Figure 3, the following finger junction dimensions were targeted:

$$5\text{ nm} \le t \le 100\text{ nm}, \quad (1)$$
$$10\text{ nm} \le w \le 100\text{ nm and} \quad (2)$$
$$200\text{ nm} \le l \le 400\text{ nm}. \quad (3)$$

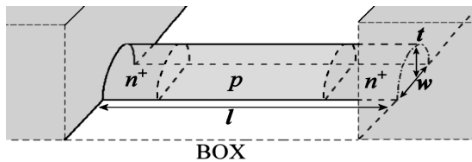

Figure 3: Generalized SOI finger junction dimensions.

Manufacturing larger rectangular Si structures and selectively oxidizing these created the desired thinner Si fingers. Nanometre-scale Si wires had already been manufactured through oxidation [12], but *pn*-junctions had, to our knowledge, never been implemented inside such thin Si wires.

1.4. Punch-through EL enhancement

Figure 4 shows two heavily doped p^+ end regions spaced a distance W_P apart by a lower doped *n*-type drift region.

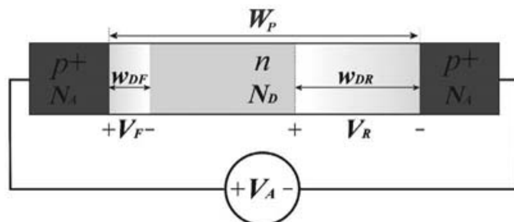

Figure 4: Punch-through variable definitions.

The applied voltage V_A can be increased to the punch-through voltage V_{PT} where the expanding reverse bias depletion region reaches the forward-biased depletion region so that $w_{DF} + w_{DR} = W_P$. At punch-through, the lowered energy barrier of the forward-biased junction injects a larger thermionic hole current that makes more minority carriers in the reverse-bias depletion region available for avalanche multiplication and radiative recombination. Achieving a higher avalanche current at lower terminal voltage also implies that the power efficiency of a punch-through light source is higher than the power efficiency of a single avalanching *pn*-junction.

2. PHYSICAL AND OPTICAL SIMULATION

Simulations were useful during the design stage to predict physical and optical properties achievable at the end of the manufacturing process.

2.1. Impurity redistribution during oxidation

The low diffusivity and solubility of arsenic (As) in SiO_2 results in the “snow-shovel” effect that causes As to pile up against the moving SiO_2 boundary during thermal oxidation [13]. Boron (B) with its higher diffusivity and solubility in SiO_2 is absorbed into the SiO_2 during thermal oxidation, therefore decreasing its concentration in the Si [14]. Since the lower B background doping concentration of n^+p junctions plays a larger role in determining junction characteristics like depletion region width w_d than the higher As concentration, only the spatial B concentration variation with thermal oxidation was further considered. The SOI B concentration $C(y,t)$ as a function of distance y from the BOX-Si interface and oxidation time t during thermal oxidation can be expressed as [14]

$$\frac{C(y,t)}{N_B} = 1 - \frac{\frac{k-m}{2}\sqrt{\frac{B\pi}{D_B}}\left\{\operatorname{erfc}\left(\frac{l - m\sqrt{Bt} - y}{2\sqrt{D_B t}}\right) + \operatorname{erfc}\left(\frac{l - m\sqrt{Bt} + y}{2\sqrt{D_B t}}\right)\right\}}{1 - e^{-\left(\frac{l-m\sqrt{Bt}}{\sqrt{D_B t}}\right)^2} + \frac{k-m}{2}\sqrt{\frac{B\pi}{D_B}}\left\{1 + \operatorname{erfc}\left(\frac{l - m\sqrt{Bt}}{2\sqrt{D_B t}}\right)\right\}} \quad (4)$$

where:

- m ≈ 0.44 is the ratio of Si removed to SiO_2 thickness grown during oxidation,
- B = parabolic SiO_2 growth-rate constant,
- D_B = B diffusion constant,
- l = initial SOI active layer thickness,
- k = C_{SiO2}/C_{Si} is the segregation coefficient,
- C_{SiO2} = B concentration on the SiO_2 side of the Si/SiO_2 boundary,
- C_{Si} = B concentration on the Si side of the same interface.

Figure 5 shows the simulated B concentration decrease from the initial implanted concentration during successive oxidations. Prior knowledge of oxidation steps therefore allowed specifying the initial B implantation dose so that the desired final average finger background B concentration of about 10^{17} cm^{-3} would be achievable. In reality, some B segregation and re-diffusion into the Si also occurs at the BOX interface, but was ignored in the simulation shown in Figure 5.

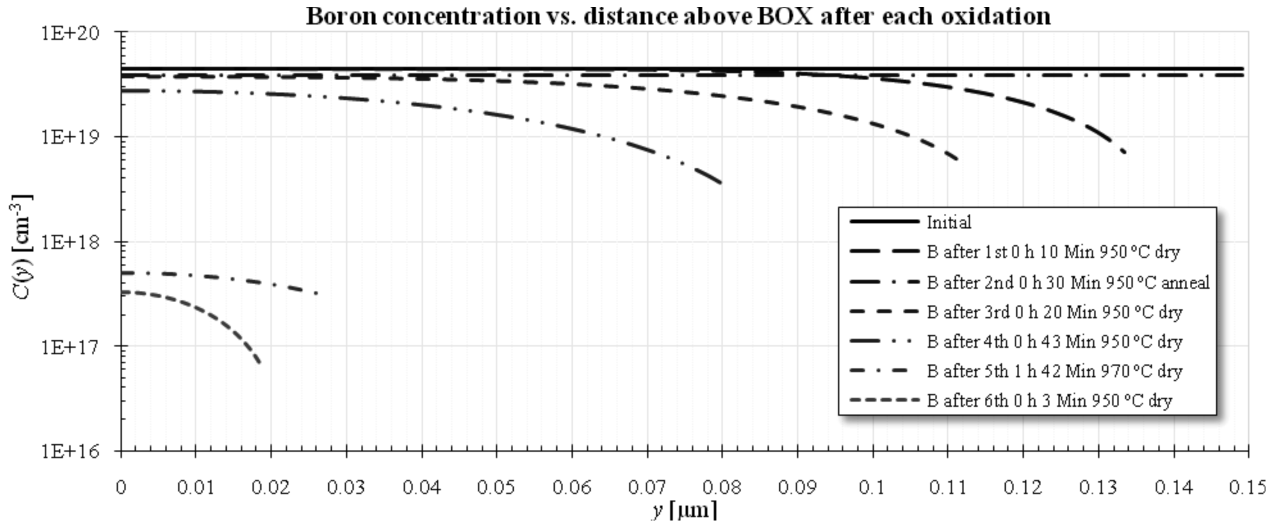

Figure 5: Boron redistribution during thermal oxidation and anneal processing steps.

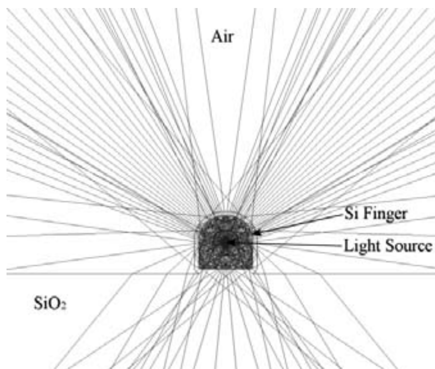

Figure 6: Simulated SOI finger spatial light radiation.

2.2. Optical radiation simulation

Employing the geometric-optical IME RAYTRACE ray-tracing software enabled the simulation of spatial light radiation characteristics of the Si fingers with varying finger geometries and light source locations.

Figure 6, for example, shows how light generated at the centre of a finger with rounded corners focuses into four lobes (recognizable by higher ray density) emanating from the rounded top surface of the Si finger.

It was *inter alia* determined that the maximum useful light emission directed away from the chip surface is achieved with a hemispherical round top finger surface to minimize internal reflection beyond the critical interface incidence angle and a flat bottom surface to maximize reflection back to the top surface.

3. DESIGN

3.1. Lithography

As indicated in Table 1, the small geometries and precise pattern alignment of the current work required electron-beam lithography (EBL), but the single beam EBL scan exposure is too slow to write all features across wafers. Hence a photolithographic mask aligner was used for patterning large-area geometries while a JEOL JBX-9300FS EPG was used for defining fine lines accurately.

Table 1: Photolithography and EBL Comparison.

Aspect	Photolithography	EBL
Wavelength/spot-size	≈ 300 nm	≈ 2 nm
Minimum feature size	≈ 0.5 µm	≈ 6 nm
Alignment accuracy	> 1 µm	> 6 nm
Wafer exposure speed	Whole wafer at once Fast: Minutes	Serial scanning beam Very slow: hours

3.2. 2D-confined SOI finger light sources

Figure 7 defines the dimensions of the pre-oxidized avalanche and punch-through SOI finger light sources.

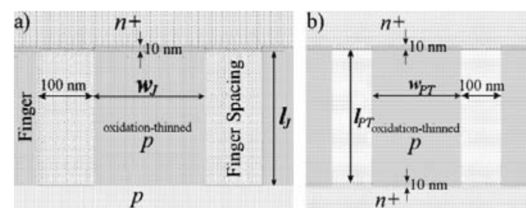

Figure 7: a) Avalanche and b) punch-through finger layout dimensions.

The Si island regions above and below the fingers remained thick while an EBL-written oxidation mask opening across the fingers allowed selective oxidation thinning of the SOI fingers. The dimensions of the devices shown in Figure 7 had to comply with the following specifications to ensure proper functionality:

$$l_J \geq w_d + d_{Ox} + 3\Delta R_{\perp As} \approx 226 \text{ nm} \quad (5)$$

$$l_{PT} \approx w_d + 2(d_{Ox} + 3\Delta R_{\perp As}) \approx 352 \text{ nm} \quad (6)$$

$$w_J = w_{PT} \approx 2t_{Si} \quad (7)$$

where

w_d = reverse bias depletion region width at breakdown,

d_{Ox} = maximum As oxidation diffusion after implant,
$\Delta R_{\perp As}$= transverse As implantation straggle,
t_{Si} = initial Si thickness (100 nm - 150 nm).
Relations (5) and (6) ensured that the fingers were long enough to accommodate the complete depletion region width after the implanted As (with its horizontal implant straggle) has diffused into the fingers after oxidation while equation (7) aimed to create semi-circular round fingers by assuming isotropic finger shaping oxidation that would thin the Si fingers equally from all sides. Implemented finger dimensions are listed in Table 3. The 30 µm x 34 µm SOI light source layout in Figure 8 depicts how 100 fingers are placed in parallel between thicker and larger Si islands that allow electrical biasing through the interconnect metallization.

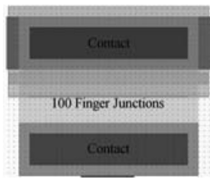

Figure 8: 100-finger junction device layout.

4. MANUFACTURE

Table 2 summarizes the processing steps and equipment involved in the SOI light source manufacture.

Table 2: Process flow overview.

Step	Action	Equipment	Graphical representation
1	Si thinning	Furnace, Reflective spectrometer	p^- Si ≈ 150 nm, BOX, Handle
2	Blanket B implant	Ion implanter	p Si, BOX, Handle
3	Si island definition	PECVD, Mask aligner, RIE	Si Island, BOX, Handle
4	As implant	PECVD, EPG, Mask aligner, RIE, Ion implanter	n+, p, BOX, Handle
5	Finger definition	EPG, RIE	n+, p, BOX
6	Finger oxidation	PECVD, EPG, Furnace	SiO_2, n+, p, BOX
7	Metallization	PECVD, Mask aligner, Sputterer	Al, Al
8	Si isolation spacing	Mask aligner	n+, p, BOX

Since no standard process recipe was employable, the complete manufacturing process had to be designed on self-obtained equipment characterization data, material and chemical properties. Consistent results and acceptable manufacturing performance were ensured through process control and monitoring that employed simultaneous processing of monitor wafer pieces and measurement of on-chip test-structures that could be analyzed with a SEM, a reflective spectrometer (to measure thin film thicknesses) and a profilometer.

Figure 9 shows examples of three final SOI finger junction dimension achieved after finger thinning oxidation.

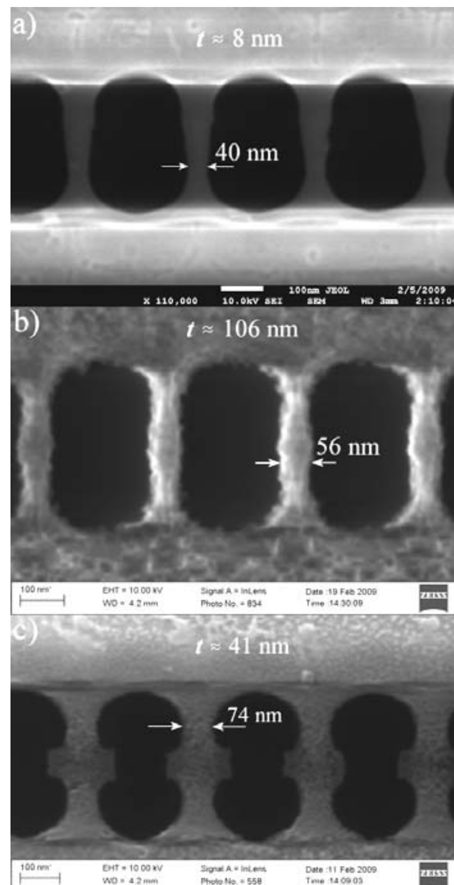

Figure 9: a) and b) avalanche and c) punch-through SOI finger final dimension examples after thinning oxidation with interpolated finger thickness estimates.

The finger thickness shown in Figure 9 are interpolated estimates from oxidation monitor island measurements. In contrast to the broad, but thin fingers in Figure 9 a), the fingers in Figure 9 b) are more thick than narrow. The punch-through SOI fingers in Figure 9 c) clearly shows how the heavily As doped Si oxidized faster than the lightly doped background. This oxidation effect created a drift and recombination region that is slightly larger than the heavily doped contact region, which should result in higher useful light emission from the light source since less light is lost due to internal reflection along the finger axis. Table 3 lists the on-mask and measured final SOI finger dimensions.

Table 3. Achieved SOI Finger Device Dimensions.

Dimension	Layout	Measured
l_J	230 nm	296 – 359 nm
w_J	200 nm – 300 nm	38 nm – 101 nm
l_{PT}	320 nm – 11 µm	348 nm – 11 µm
w_{PT}	220 nm – 12 µm	30 nm – 11.9 µm

5. MEASUREMENT

Table 4 and Figure 10 depict the finger dimensions and measured electrical characteristics of punch-through light sources selected for comparative optical characterization.

Table 4. Selected SOI light source finger dimensions.

Device	w_{PT}	l_{PT}
D1b	11.9 µm	11.8 µm
D2b	11.9 µm	11 µm
D4b	5.9 µm	4 µm
D5b	5.9 µm	4 µm
n1b	485 nm	240 nm
n2b	385 nm	240 nm

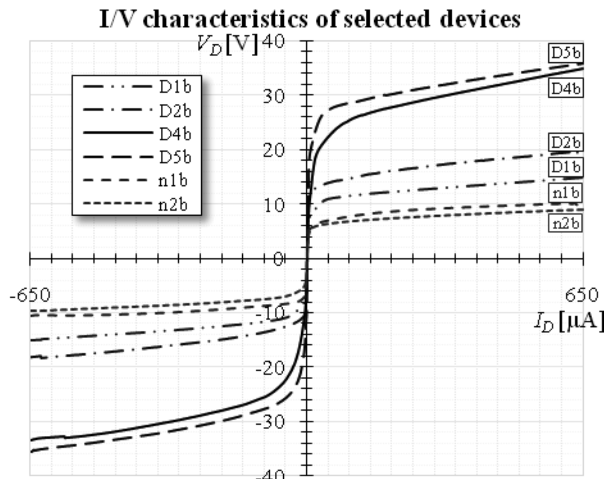

Figure 10: I-V characteristic of selected SOI light sources.

D4b and *D5b* should have high light generation efficiencies, since a higher series resistance corresponds to a thinner Si device layer and an increased breakdown voltage is characteristic of quantum-confinement.

Figure 11 shows the light generation of fingered punch-through SOI light source *n1b* at 650 µA.

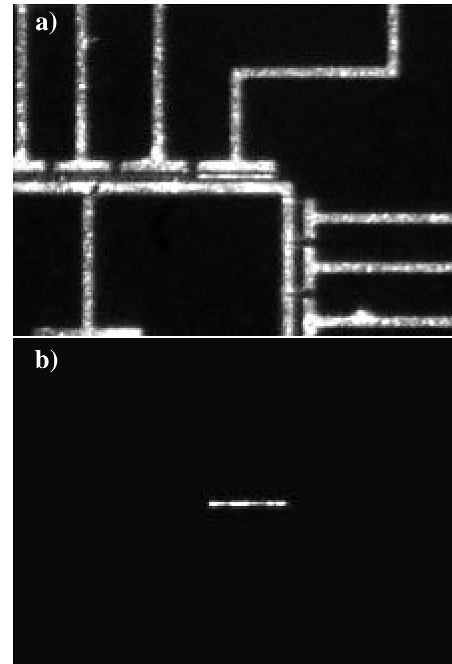

Figure 11: a) Illuminated and b) non-illuminated light generation of punch-through SOI light source *n1b*.

Figure 12 compares the spectrum of the SOI punch-through light source with the highest optical power (*D4b*) to the average optical power of 0.35 µm avalanche CMOS light sources also biased at I_D = 650 µA and measured with the same characterization setup. While the avalanche light sources peak around $\lambda \approx 660$ nm ($E_{Ph} \approx$ 1.88 eV) the SOI punch-through light source peak around 850 nm ($E_{Ph} \approx 1.46$ eV) is about 9 times higher. Since significant infrared radiation peaks were observed in Si nano-crystal EL and photoluminescence experiments [15], this could be indicative of quantum confinement. The lower photon energy at longer wavelengths also implies that that the thickness-confined SOI light sources have significantly higher quantum conversion efficiencies than bulk-CMOS avalanche light sources.

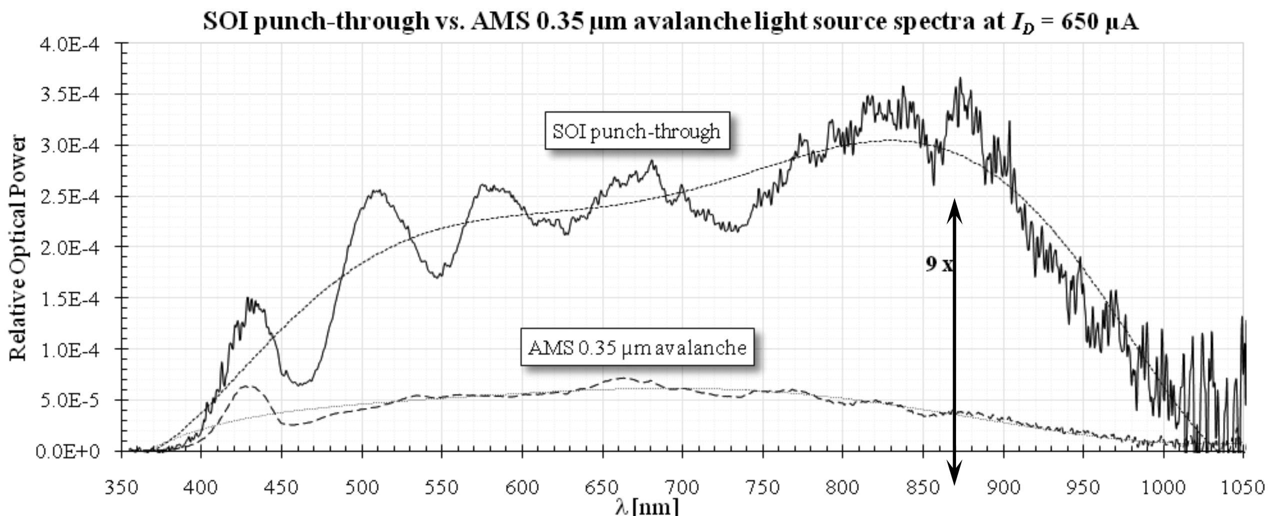

Figure 12: Spectra comparison of SOI punch-through and AMS 0.35 µm CMOS light-sources.

The periodic optical power variation of all measured SOI light sources is due to light reflection off the SiO_2 BOX layer covering the SOI wafer Si handle. Employing the stack transmission model, the best-fitting simulated Si-SiO_2-air stack reflection peaks were achieved for $t_{BOX} \approx$ 860 nm (Figure 13).

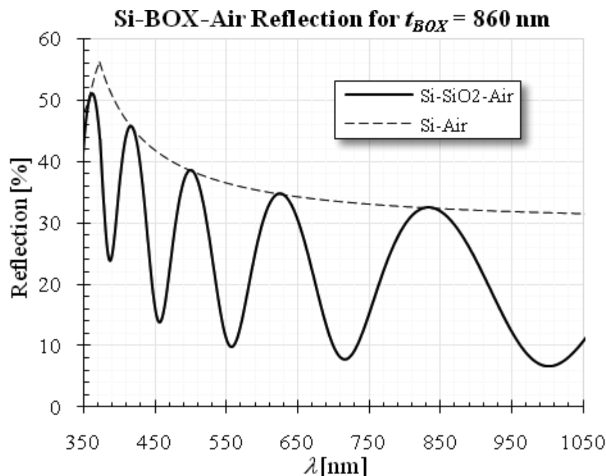

Figure 13: Simulated BOX reflection for t_{BOX} = 860 nm.

Figure 13 shows that an average of 25 % of the light that would have been lost through downward radiation is reflected back up as useful light.

6. CONCLUSION

All measured thickness-confined SOI light sources displayed a pronounced optical power for $0.6 < \lambda < 1$ µm. The SOI light source with the highest optical power output emitted about 9 times more optical power around λ = 850 nm than a 0.35 µm bulk-CMOS avalanche light-source operating at the same current. It has also been shown that the BOX layer in a SOI process could be used to reflect about 25 % of the light that would usually be lost to downward radiation back up, thereby increasing the external power efficiency of SOI light sources.

7. REFERENCES

[1] L Chao, *Intel Technology Journal*, Vol. 8, Issue 2, 10 May 2004, ISSN 1535-864X.

[2] R Newman, WC Dash, RN Hall and WE Burch, "Visible light from a Si p-n junction", *Phys. Rev.*, Vol. 98 A, 1955, pg. 1536.

[3] A Chatterjee, B Bhuva and R Schrimpf, "High-speed light modulation in avalanche breakdown mode for Si siodes", *IEEE Electron Device Letters*, Vol. 25, No. 9, September 2004, pg. 628.

[4] A Chatterjee and B Bhuva, "Accelerated stressing and degradation mechanisms for Si-based photoemitters", *IEEE Transactions on Device and Materials Reliability*, Vol. 2, No. 3, September 2002, pg. 60.

[5] SK Tewksbury, *Semiconductor Materials*, Microelectronic Systems Research Center, Dept. of Electrical and Computer Engineering, West Virginia University, Morgantown, WV, 21 Sept. 1995, pg. 12.

[6] M du Plessis, H Aharoni, and LW Snyman, "Spatial and intensity modulation of light emission from a silicon LED matrix", *IEEE Photonics Technology Letters*, Vol. 14, No. 6, June 2002, pg. 768.

[7] M du Plessis, H Aharoni and LW Snyman, "Two- and multi-terminal CMOS/BiCMOS Si LEDs", *Optical Materials*, Vol. 27, 2005, pp. 1059 - 1063.

[8] T Hoang, P LeMinh, J Holleman and J Schmitz, "Strong efficiency improvement of SOI-LEDs through carrier confinement", *IEEE Electron Device Letters*, Vol. 28, No. 5, May 2007, pg. 383.

[9] H Tu, *High efficient infrared light emission from silicon LEDs*, Doctor degree dissertation at the University of Twente, ISBN 978-90-365-2557-2, Wöhrmann print service, Zutphen, The Netherlands, 2007, pg. 105.

[10] S Saito, D Hisamoto, H Shimizu, H Hamamura, R Tsuchiya, Y Matsui, T Mine, T Arai, N Sugii, K Torii, S Kimura and T Onai, "Electro-luminescence from ultra-thin silicon", *Japanese Journal of Applied Physics*, Vol. 45, No. 27, 2006, pp. L679-L682.

[11] A Karsenty, A Sa'ar, N Ben-Yosef and J Shappir, "Enhanced electroluminescence in silicon-on-insulator metal-oxide-semiconductor transistor with thin silicon, *Applied Physics Letters*, Vol. 82, No. 26, June 2003, pg. 4830.

[12] D Shir, BZ Liu, AM Mohammad, KK Lew and SE Mohney, "Oxidation of silicon nanowires", *J. Vac. Sci. Technol. B*, Vol. 24, No. 3, May/June 2006, pg. 1333.

[13] GA Tarnavskii, SI Shpak and MS Obrecht, "Features of segregation of doping impurities of V(a) subgroup elements on angular configurations of the silicon/silicon dioxide oxidation boundary", *Journal of Engineering Physics and Thermophysics*, Vol. 75, No. 1, 2002, pg. 190.

[14] Z Đurić, MM Smiljanić, K Radulović and Z Lazić, "Boron redistribution during SOI wafer thermal oxidation", Proc. 25th *International Conference on Microelectronics (MIEL 2006)*, Belgrade, Serbia and Montenegro, 14 – 17 May 2006.

[15] K Chen, J Huang, Z Ma, X Wang, Y Yao, J Wang, W Li, J Xu and X Huang, "Charge storage and light emission properties of three dimension controllable Si nanostructures", *Phys. Status Solidi*, Vol. C6, No. 3, 2009, pp. 721 – 727.

A FULLY CMOS OPTICAL TRANSMISSION SYSTEM BASED ON LIGHT EMITTING AVALANCHE DIODES

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Abstract: The successful realization of optical interconnects for inter- and intra-chip communication strongly depends on the use of a light source that is compatible with existing, well established manufacturing processes – primarily CMOS/VLSI. The problematic integration of III-V light sources with CMOS technology has not been surmounted thus far. While silicon is ill-suited as an optical material, silicon based light sources present a huge advantage: complete monolithic integration using existing CMOS processes. This advantage can only be exploited if these devices show sufficient switching speed and optical power emission to make high speed clock and data transmission feasible. This paper illustrates the switching speed of silicon based light emitting devices in excess of 100 MHz and the viability of using such a device for an all-silicon optical link for clock and data distribution.

Key words: Optical interconnect, silicon light emission, silicon photonics.

1. INTRODUCTION

As CMOS component feature sizes are constantly being scaled down, delay degradation and power dissipation in metal interconnects will remain problematic. In the International Technology Roadmap For Semiconductors (ITRS)-2007 [1] it is predicted that optical interconnects could become one of the most viable alternative solutions to improve device and systems-on-a-chip solution performances, as the down-scaling continues.

The industry has used III-V light emitters for optical communication, over long distances, because of their high quantum efficiencies. However, the relatively short distances involved in inter- and intra-chip optical interconnects require much less optical power. This makes less efficient on-chip silicon light sources a viable alternative in the above mentioned application fields [2]. It is also well documented that silicon light emitting diodes normally have low light emitting efficiencies, but if the latter can be optimized [3], it can be utilized effectively in all–silicon optical interconnect solutions [4].

This paper will highlight the fact that even with relatively low effective power efficiencies (EPE), of the order of 10^{-6}, the p-n silicon light sources designed and developed to operate in the reversed bias avalanche mode [5], could be modulated at clock frequencies of up to 120 MHz. The only restriction lies in the fact that the detector circuit was band limited to 100 MHz.

Furthermore data transfer rates of up to 700 kbps were obtained between chips, with relatively low optical power output of the silicon light source, the main limitation.

2. SILICON LIGHT SOURCE

2.1 Point source description

The light sources consist of a reverse biased *pn*-junction formed in bulk silicon in a standard CMOS process. *n*+ structures are defined such as to enhance current density for illuminating a single concentrated point with submicron dimensions. A number of these point sources are stacked into an array and then modulated off chip by switching the devices at the boundary of avalanche breakdown. The devices break down at around 9 V, where the voltage across the devices is biased just below this value. Pulsed currents are then used to cause avalanche emission in the devices, resulting in a usable optical signal for transmission.

2.2 Reflectors

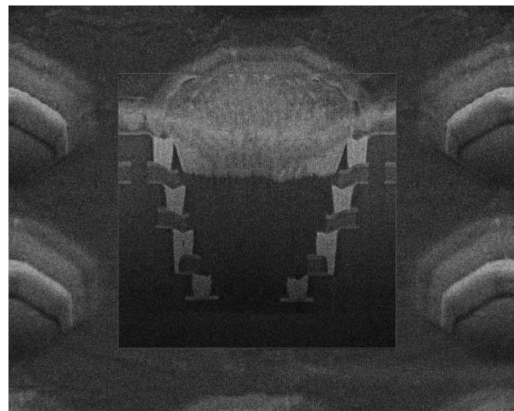

Figure 1: Cross section of reflector structure as seen under scanning electron microscope (SEM).

Figure 1 shows the light directing reflector structures used to further enhance the amount of light available perpendicularly to the light sources. Since the fibre is mounted orthogonally to the substrate plane, the reflectors assist in coupling stray light into the fibre, which improves the overall external power efficiency of the source.

3. SWITCHING SPEED

3.1 Si diode light modulation

Silicon light emitting diodes operating in avalanche breakdown have been shown to allow light modulation up to 20 GHz using streak camera tests [6] with emission resulting from hot carrier luminescence [7]. These results prove that the modulation speed of light emitting silicon diodes in avalanche breakdown is not limited by the underlying physical processes but rather the electrical bandwidth of supporting circuitry and devices.

In this paper the high speed switching capability of Si light emitting devices is measured electrically – requiring an optical-electrical conversion – which also shows that the recovery of a useful electrical signal is possible.

3.2 Experimental setup

The experimental setup is shown (conceptually) in Figure 2. A function generator (Agilent 33250A) was used to generate a sinusoidal signal to serve as an input to a driver circuit that modulated the current through the light emitting diode. The driver circuit – an emitter coupled transistor pair – was built using discrete components. The on-chip silicon light source was aligned to an optical fibre in a makeshift manner. The specifications of the optical fibre are given in Table 1.

At the receiver end, the fibre was directly connected to a commercial silicon avalanche photo diode (APD) module (detailed in Table 2). The voltage output of the APD module was connected to a spectrum analyzer (Rohde & Schwarz FSP).

A spatial separation of ~13 m between the transmitter and the receiver was used to limit the influence of electromagnetic coupling. To verify that the signal measured by the spectrum analyzer was indeed optical, measurements were taken both with and without the optical fibre connected to the APD module. This is illustrated in Figure 3 for a transmitted 120 MHz clock signal. The optical signal is clearly distinguishable over the noise floor.

The detection of clock signals at higher frequencies is primarily limited by the bandwidth of the APD module currently used which has a -3 dB bandwidth of 100 MHz.

The successful transmission and detection of a clock signal in the GHz range will require a faster APD module, improved driver circuitry (likely to be integrated on-chip) and a mechanism to limit bandwidth integrated noise.

Table 1: Specifications for Thorlabs BFL-600 low OH optical fibre.

Length	15 m
Core diameter	600 µm
Numerical aperture	0.37 N.A.
Type	Multimode
Spectral range	400 nm – 2200 nm
Attenuation	0.01 – 0.1 dB/m

Table 2: Specifications for Hamamatsu silicon APD module C5331-11.

Bandwidth	4 kHz – 100 MHz
Photoelectric sensitivity	$\sim 2.5\text{x}10^4$ V/W
Active diameter	1.0 mm
Peak sensitivity (Si APD)	0.42 A/W @ 620nm

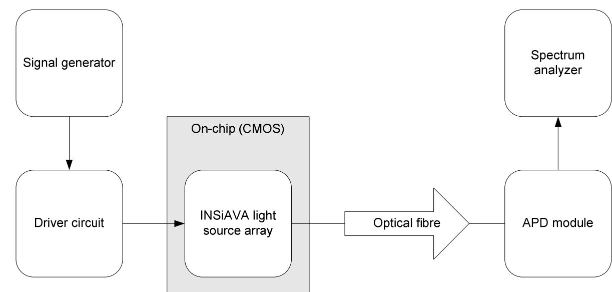

Figure 2: Conceptual experimental setup for optical clock transmission and measurement at the receiver.

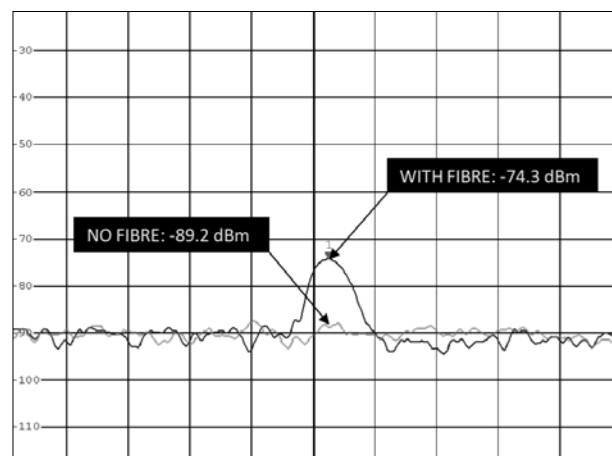

Figure 3: Measured spectrum of a 120 MHz clock signal with and without the optical fibre connected to the APD module.

4. DATA LINK

To illustrate the viability of using silicon light sources for data transmission, a simple baseband modem was designed to operate at a data rate of 176 kbps. A conceptual overview of the optical data link is shown in Figure 4.

4.1 Experimental setup

With reference to Figure 4: A pseudo random binary signal generator (T.1) was used as a data source. The voltage of the corresponding non-return-to-zero (NRZ) encoded data was appropriately adjusted (T.2) and fed to the driver circuit (T.3) to modulate the current of the light emitting device (T.4).

A 15 m optical fibre was once again coupled to the light source. At the receiving end the APD module (R.1) converts the optical signal to a voltage. The magnitude of this voltage signal is not large enough to be displayed on an oscilloscope; it must first be amplified (R.2) before further signal processing steps may be performed on it. After amplification the signal is passed through a Nyquist filter (R.3). The filtered signal is fed to a comparator (R.4) which hard-limits the signal to digital voltage levels (0-5 V). The embedded clock is recovered (R.5) from the NRZ encoded data, which is then used to re-time (R.6) the digital data signal.

The clock recovery, as illustrated in Figure 4, was performed in a conventional manner by performing a non-linear operation (R.5.1) on the signal to generate a spectral component at the clock frequency unto which the phase-locked loop (R.5.3) can lock. A monostable multivibrator (R.5.2), configured to be non-retriggerable, is triggered by the pulses from the zero-crossing detector (R.5.1) to ensure consistently shaped pulses. A delay element is added to adjust the clock phase to ensure the data signal is sampled at the optimal time instant i.e. in the middle of the 'eye'.

Figure 5 shows an eye diagram with a 176,000 baud rate and 35 mV_{p-p} amplitude. The evident spikes are caused by the switching noise of the oscilloscope's trigger signal. With the use of high speed current feedback operational amplifiers (AD8011), this symbol rate was quadrupled to 704,000 baud (as shown in Figure 6). However, further signal processing steps (i.e. R.4 to R.6) were not implemented at this symbol rate.

4.2 CMOS integration

The discussed system was built using only commonly available integrated circuits (mainly from the 4000 CMOS logic family). The employed APD module also uses a silicon APD. Thus, the entire system could be implemented, using a CMOS process, in a single integrated circuit.

Optical receiver front-end designs, using standard CMOS processes, have been reported [8]-[10] most recently operating up to 10 Gbps [11]. The design of high speed CMOS driver circuits for vertical cavity lasers, operating at 10Gbps, have also been shown [12]. Similar designs could be used to drive Si diodes [2] instead of III-V light sources. This all implies that a 10 Gbps optical interconnect, using only CMOS technology, is definitely feasible if the present power efficiency of silicon light sources can be further improved.

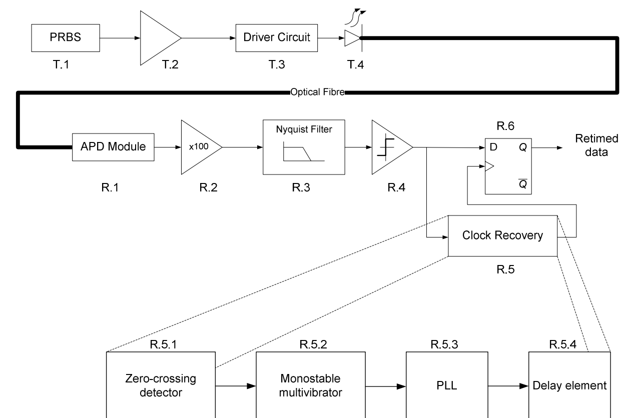

Figure 4: Conceptual overview of baseband modem for all-silicon optical data link.

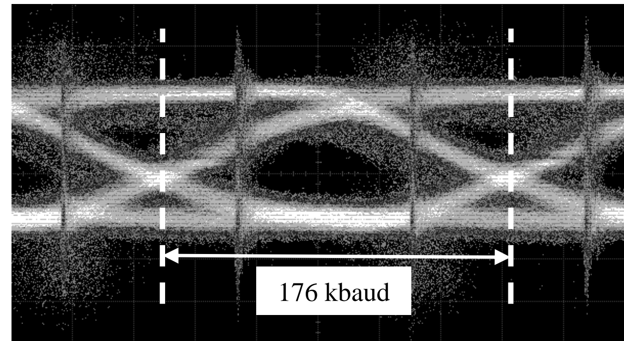

Figure 5: Eye diagram showing a symbol rate of 176 kbaud with an amplitude of 35 mV_{p-p}.

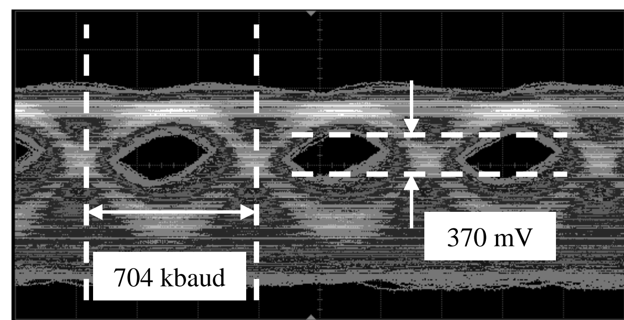

Figure 6: Eye diagram showing a symbol rate of 704 kbaud with a vertical eye opening of 350 mV.

5. CONCLUSION

The modulation of a VLSI-compatible silicon light emitting device has been successfully shown up to 120 MHz, primarily limited by the bandwidth of the APD module used. Furthermore, a fully functional, CMOS based, inter-chip optical interconnect operating at 176 kbps proves the feasibility of using an all-silicon solution for data and clock distribution. With increased EPE of silicon light emitters, the realization of a 10 Gbps optical interconnect should be feasible.

6. REFERENCES

[1] International Technology Roadmap For Semiconductors (ITRS). Semiconductor Industry Association, 2007 Edition.

[2] S. Sayil, “Avalanche breakdown in silicon devices for contactless logic testing and optical interconnect”, *Analog Integrated Circuits and Signal Processing,* vol. 56, pp. 213-221, 2008.

[3] M. du Plessis, H. Aharoni and L. W. Snyman: "Silicon LEDs fabricated in standard VLSI technology as components for all silicon monolithic integrated optoelectronic systems", *IEEE Journal on Selected Topics in Quantum Electronics,* vol. 8, pp. 1412-1419, 2002.

[4] A. Chatterjee, P. Mongkolkachit, and B Bhuva, “ All Si-based Optical Interconnect for Interchip signal transmission”, *IEEE Photonics Technology Letters,* vol. 15, No. 11, pp. 1663-1665, 2003.

[5] M. du Plessis, H. Aharoni and L. W. Snyman, " Two and multi-terminal silicon light emitting devices in standard CMOS/BiCMOS IC technology” *Physica Status Solidi (a)*, vol. 201, No.10, pp. 2225-2233, 2004.

[6] A. Chatterjee, B. Bhuva and R. Schrimpf, “High-speed light modulation in avalanche breakdown mode for Si diodes”, *IEEE Electron Device Letters, vol. 25, No. 9, pp.* 628-630, 2004.

[7] J. C. Tsang and J. A. Kash, Picosecond hot electron light emission from CMOS circuits. *Applied Physics Letters*, vol.70, No. 7, pp 889-891, 1997.

[8] C. Hermans and M. S. J. Steyaert, "A high-speed 850-nm optical receiver front-end in 0.18-μm CMOS," *IEEE Journal of Solid-State Circuits,* vol. 41, pp. 1606-1614, August 2006.

[9] Sung Min Park, Jaeseo Lee and Hoi-Jun Yoo, "1-Gb/s 80-dBΩ; fully differential CMOS transimpedance amplifier in multichip on oxide technology for optical interconnects," *IEEE Journal of Solid-State Circuits,* vol. 39, pp. 971-974, May 2004.

[10] W. Chen, Y. Cheng and D. Lin, "A 1.8-V 10-Gb/s fully integrated CMOS optical receiver analog front-end," *IEEE Journal of Solid-State Circuits,* vol. 40, pp. 1388-1396, March 2005.

[11] S. Palermo, A. Emami-Neyestanak and M. Horowitz, "A 90 nm CMOS 16 Gb/s transceiver for optical interconnects," *IEEE Journal of Solid-State Circuits,* vol. 43, pp. 1235-1246, April 2008.

[12] S. Rabii *et al.*, “An integrated VCSEL driver for 10Gb/s Ethernet in 0.13μm CMOS,” *ISSCC Digest of Technical Papers*, pp. 246-247, San Francisco California, Feb. 2006.

CHARACTERISATION OF ADAPTIVE FLUIDIC SILICONE-MEMBRANE LENSES

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Abstract: We compare the performance and optical quality of two types of adaptive fluidic silicone-membrane lenses. The membranes feature either a homogeneous thickness, or they are shaped resulting in an inhomogeneous cross-section. The lens systems incorporate a piezoelectric actuator which is operated in a regime of ±40 V. The shaped membrane lenses show lower wave front errors than the planar ones, down to 24 nm. The pumping actuator indicates a maximum pump volume of 1159 nl at an inner piezo radius of 2.75 mm for the smallest supporting ring configuration. The full system with a planar membrane achieves a larger refractive power ranging from +19 to -14 dpt. It also shows a shorter full scale response time (t_{planar} = 23.9 ms) compared to the shaped membrane (t_{shaped} = 35.4 ms).

Key words: adaptive optics, piezoelectric actuator, silicone

1. INTRODUCTION

The development of adaptive lenses increased drastically over the last few years. In contrast to conventional systems with mechanical moving parts, adaptive lenses show no mechanical wear, however they are costly. In the meantime, three lenses based on different working principles are commercially available. The first one is the electrowetting lens of Varioptics. The lens with a clear aperture of 2.5 mm is developed for the main application in consumer electronics (mobile phones, PDAs, laptops) [1]. The second lens of Optotune has an aperture of 6 mm in diameter and is mostly suitable for digital cameras and microscopes. The adaptive lens is based on an electroactive polymer, which deforms an elastic lens [2]. The third product is available at Holochip and consists of a fluid-based singlet lens, where the interface is set by an elastic silicone membrane. The focal length of the lens with an aperture of 10 mm is tunable by the mechanical moving of the clamping ring [3].

As an alternative to the commercially available lenses we have recently presented an adaptive silicone membrane lens with an integrated piezoelectric pump for actuation. The lens is suitable for the use in optical systems with a clear aperture of 2.5 mm [4, 5]. In this paper we focus on the characterisation of the single components (lens and pump actuator) and the full system for lenses with planar and shaped membranes.

2. ASSEMBLY AND FABRICATION

The system consists of two components: a lens and a pump actuator, which are connected via a glass substrate (see figure 1). The lens chamber is filled with water or immersion oil, and consists of a silicone membrane with a homogeneous or an inhomogeneous thickness, and of a supporting ring (see figure 2).

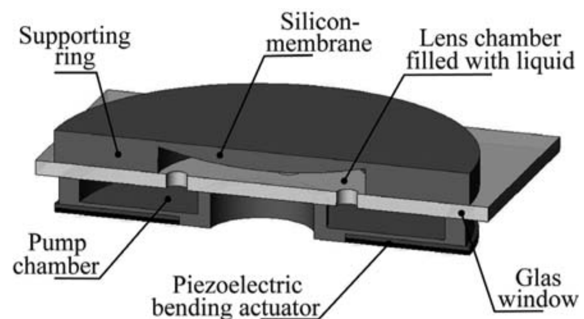

Figure 1: Adaptive liquid lens with an integrated piezoelectric actuator.

The pump chamber, which is also filled with liquid, is made up of a piezoelectric bending actuator embedded in silicone. The exchange of liquid between the pump and lens chamber is enabled by orifices in the glass substrate. If a voltage is applied to the piezo-bending actuator, its interior bulges upwards so that the lens fluid is displaced from the pump chamber into the lens chamber. This causes a growing bulge of the lens membrane and thus a reduction in the focal length of the lens.

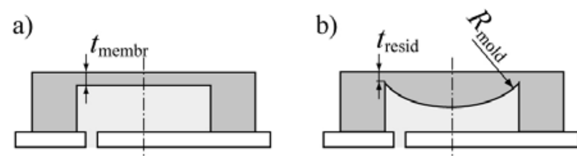

Figure 2: Membrane variations, lens chamber with a) planar and b) shaped membrane.

The lens and the pump chamber are fabricated with a surface roughness of $R_a < 40$ nm in polydimethylsiloxane (PDMS). The two chambers are cast in a hot embossing machine. In the fabrication process, a brass

substrate produced by ultra-precision milling (UPM) is used as mold. Exemplarily the fabrication process of the lens chamber is shown in figure 3. In case of a homogenously thick membrane, the membrane thickness t_{membr} is controlled by a spacer ring located between the brass mold and the polycarbonate foil. Additionally, for the inhomogeneous membrane we place concave shaped lenses in the mold. Generally, the volume shrinkage of the silicone is counteracted by the stamp force during the hardening process in the hot embossing machine. Since this force, however, is constant for all membrane thicknesses, the volume shrinkage for several membrane thicknesses increases with the cube of the membrane thickness.

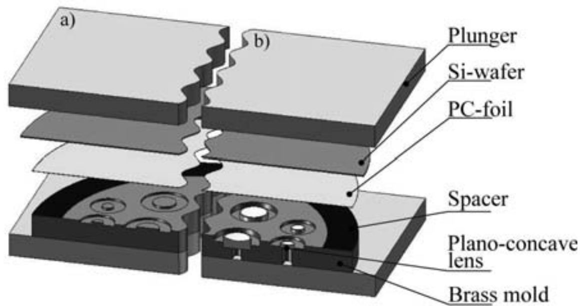

Figure 3: Fabrication process in a hot embossing machine for a lens chamber with a) a planar and b) a shaped membrane.

3. CHARACTERIZATION

This chapter is devoted to the characterisation of the single components and the full system. The simulation and measurement of the optical lens quality is realized by a FE- and ray tracing simulation and a Mach-Zehnder interferometrical setup. The pump volume of the piezoelectric bending actuator is optimized by FE-simulation and a laser-profilometer. For the full system we are analyzing the refraction power as a function of the piezo voltage and the dynamical behavior as well.

3.1 Optical lens quality

The optical lens quality of the opto-mechanical component is analyzed by a mechanical FE-simulation and ray tracing. In order to judge the lens quality, we examined the wave front error (WFE_{RMS}) of the different membrane shapes in a horizontal lens orientation. For the PDMS we set an elastic modulus of 1.54 MPa [6], a Poisson ratio of 0.49 and a refractive index of 1.4282 [6]. As lens liquid we use water with a refractive index of 1.33.

Figures 4 shows the wave front error in RMS as a function of the focal length for lenses with homogeneous membranes in horizontal orientation. Generally, the wave front error is decreasing for increasing focal length and decreasing membrane thickness. The influence of the membrane thickness is traced back to the reduction of the membrane stiffness which shifts the inflection point of the membrane in the direction of the membrane fixation, which reduces the spherical aberration. In the horizontal orientation the hydrostatic pressure of the lens fluid increases the membranes radius of curvature and decreases the spherical aberration, which results in a rising lens performance.

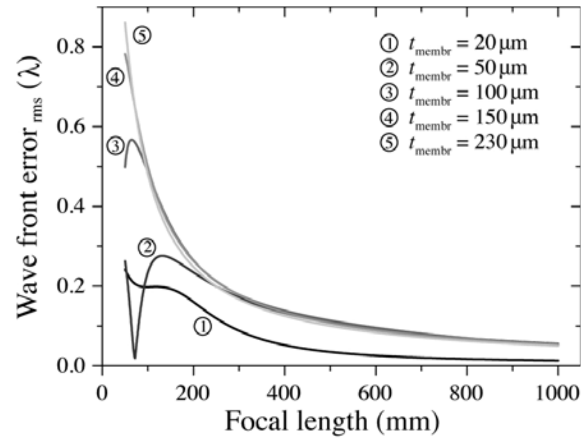

Figure 4: Simulated aberration of the planar membrane lens as a function of the focal length. d_{lens} = 5 mm, d_{ap} = 2.5 mm.

For the lenses with inhomogeneous membranes the influence of the residual membrane thickness t_{resid} (see figure 2b) at 10 mm radius of curvature R_{mold} is investigated (see figure 5). The curves show the smallest aberration in the non-deflected initial state at a focal length of 125 mm. For deflected situations (increasing or decreasing focal length) the wave front errors increase drastically with a decreasing residual membrane thickness due to a more inhomogeneous membrane deformation.

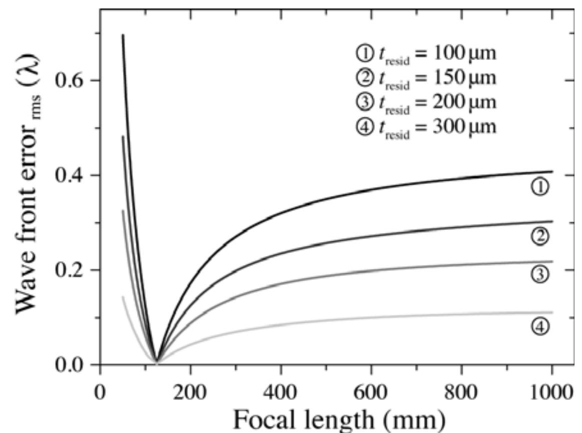

Figure 5: Simulated aberration of the shaped membrane as a function of the focal length. d_{lens} = 5 mm, d_{ap} = 2.5 mm, R_{mold} = 10 mm.

For experimental characterization of the optical lens quality we measure the wave front error (WFR_{RMS}) at a wave length of 633 nm by using a Mach-Zehnder interferometer. The detailed configuration of the interferometer is given in [7]. Figure 6 shows the

measurement results of the lenses with homogenous membranes as a function of the focal length for different membrane thicknesses at an aperture of 2.125 mm. The diagram shows a minimal wave front error in RMS of 0.047 λ for a membrane thickness of 50 µm at a focal length of 800 mm. In general, the curve shapes of the measurements and the simulations without volume shrinkage (see figure 4) are in a good correlation.

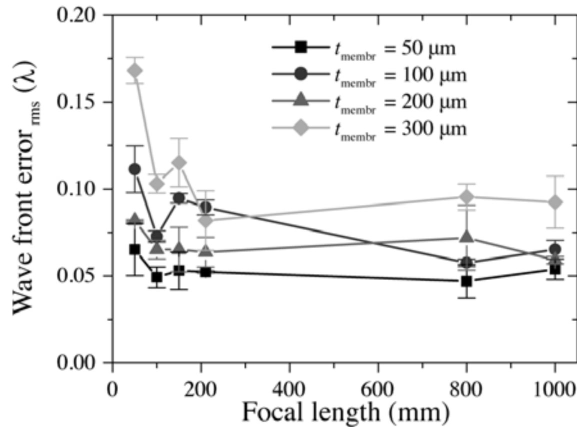

Figure 6: Measured aberration of the planar membrane lens as a function of the focal length. d_{lens} = 5 mm, d_{ap} = 2.125 mm.

Figure 7 shows the measurement result of the inhomogeneous membrane lens for diverse residual membrane thicknesses at a mold radius of curvature of 9.3 mm. All curves illustrate a minimal aberration at a focal length of 66 mm. The wave front error is increasing for decreasing membrane thickness and deflection of the membrane. In comparison to the homogeneous membrane the minimum wave front error could be reduced to 0.037 λ. The trend of the measurement curves are in good correlation to the simulated behavior without volume shrinkage (see figure 5).

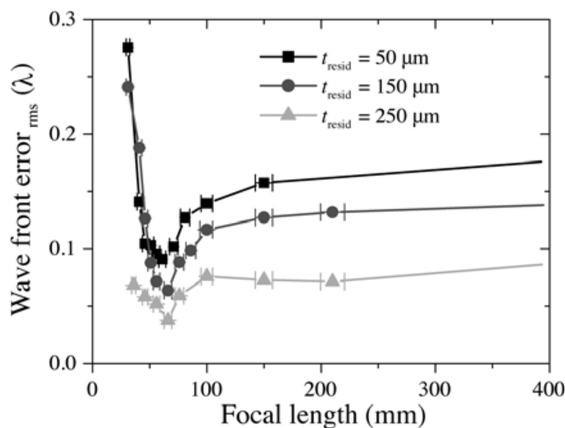

Figure 7: Measured aberration of the shaped membrane as a function of the focal length. d_{lens} = 6 mm, d_{ap} = 2.125 mm, R_{mold} = 9.3 mm.

The difference between the simulation and the measured focal length in the initial state can be traced back to the volume shrinkage of the silicone during the fabrication process which let the focal length decrease.

3.2 Pump actuator

This paragraph is devoted to the optimization of the piezoelectric pump. For this purpose we concentrate on the maximization of the pump volume by using FE-simulation. Therefore, the influence of the inner piezo radius r_{piezo} and the inner and outer supporting ring width Δr are analyzed (see figure 8).

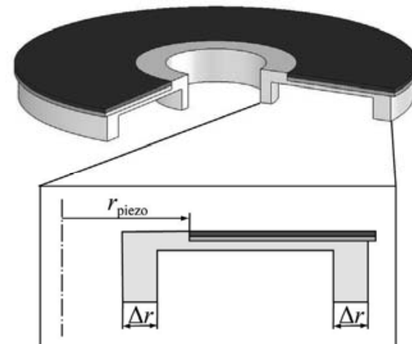

Figure 8: Parameter model of the piezoelectric pumping actuator.

Figure 9 shows the pump volume as a function of the inner piezo radius for diverse supporting ring width Δr at an applied voltage of -40 V. A maximum volume of 1405 nl is displaced at a inner piezo radius of 2810 µm for the thinnest supporting ring configuration. A reduction in the effectiveness of the pump with small inner piezo radii can be attributed to an elevated mechanical stiffness in the inner supporting ring. On the other hand, with larger radii the pump volume decreases due to the declining length of the bending actuator. The pumping volume is decreasing for increasing supporting ring width, due to the increasing stiffness of the actuator fixation.

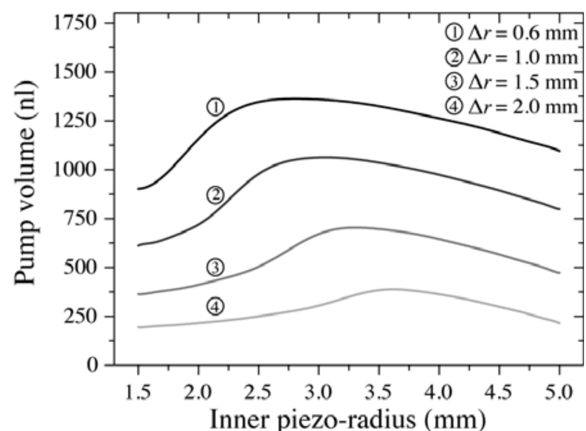

Figure 9: Simulation of the displaced pump volume as a function of the inner piezo radius r_{piezo} for diverse supporting ring width at -40 V.

The measurement of the pump volume is realized by a laser-profilometer. After a surface scan of the piezoelectric actuator at a voltage of -40 V the pump volume is calculated. Exemplarily, figure 10 shows the measurement result for a two different supporting ring widths of 600 and 1000 µm. On the one hand, the maximum pump volume for the actuator with the thinner supporting ring is 1159 nl at an inner piezo radius of 2.75 mm. On the other hand, the displaced volume for the configuration with the thicker supporting ring is decreasing down to 892 nl at a inner piezo radius of 3.25 mm. The curve shapes of the measurement and the simulation are in a good correlation. The difference in the pump volume can be traced back to the volume shrinkage of the silicone which increases the supporting ring stiffness. Otherwise, the process related internal stress in the piezoelectric bending actuator reduces the displaced volume as well.

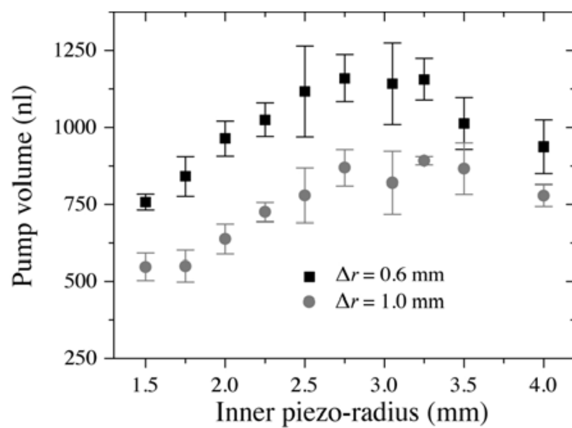

Figure 10: Measurement result of the displaced pump volume as a function of the inner piezo radius r_{piezo} for different supporting ring width Δr at -40 V.

3.3 System performance

For the full system we want to know the refraction power as a function of the piezo voltage. In the simulation the interaction of the lens chamber to the pump performance has been considered. In a first simulation step, the lens back pressure as a function of the lens volume, respecttively the focal length has been simulated. In the second step we calculated the pump volume of the actuator as a function of the piezo voltage inclusive lens back pressure in an iterative simulation. Finally, the pump volume of the actuator and the lens volume are set equal to link the focal length to the piezo voltage. Exemplarily, figure 11 shows the system performance of lenses with homogeneous membranes between a thickness of 20 and 230 µm. The maximum refraction power range is not achieved for the thinnest membrane as one would actually expect but for a medium membrane thickness of 150 µm. This is related to two opposing effects. On the one hand, the actuator simulation inclusive lens backpressure shows a decreasing pump volume for an increasing membrane thickness.

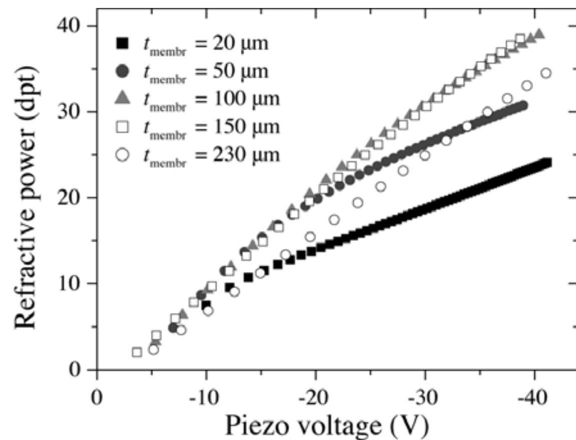

Figure 11: Simulated refractive power as a function of the piezo voltage for different homogeneous membrane thicknesses t_{membr}.

On the other hand, with decreasing membrane thickness the radius of curvature increase, as can be seen in figure 12, due to the shift of the membrane inflection point.

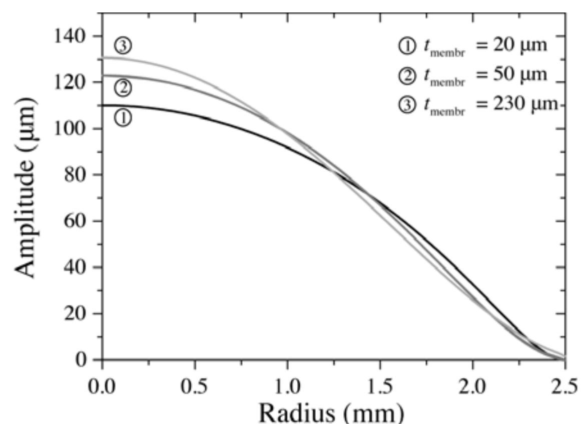

Figure 12: Simulated membrane shapes for a lens volume of 1 µl at divorce homogeneous membrane thicknesses.

The measurement of the system behaviour is realized by the laser-profilometer in the dynamic mode. For the lens with a homogeneous membrane the membrane surface profile is measured and the refraction power of the lens is calculated subsequently. Additionally, for the membranes with an inhomogeneous form the shape of the membrane backside is calculated via FE-simulation. Figure 13 displays the measured refractive power as a function of the piezo voltage at a frequency of 1 Hz. The system with the planar membrane show a refractive power range of +19 to -14 dpt, and the shape one a range of +9…+1 dpt. The reduced refractive power range of the system with an inhomogeneous lens membrane arises from the increasing membrane stiffness, respectively the increasing back pressure to the pump actuator. The big difference between the simulation result and measurements can be traced back to the volume shrinkage of the silicone which in not considered in the simulation. The hysteresis curve

shape at the measurements is typically for piezoelectric actuators.

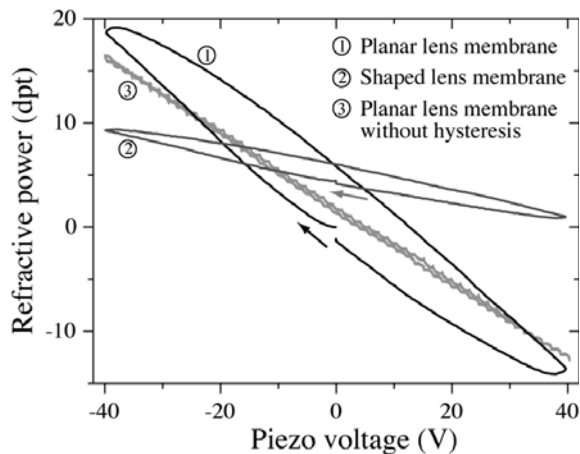

Figure 13: Measured refractive power as a function of the piezo voltage for a system with a planar (t_{membr} = 60 µm) and a shaped (t_{resid} = 75 µm, R_{mold} = 9.3 mm) lens membrane.

In order to reduce the hysteresis we operate the piezoelectric actuator dynamically. First, a piezo voltage U_{piezo} is applied to the actuator for a time of 15 ms. Afterwards, the whole hysteresis curve is run through in 60 µs. Thereby, the lens membrane can not follow the actuator movement, due to the high damping of the lens membrane. Exemplarily, figure 13 also shows the drastic hysteresis reduction for the lens with a homogeneous membrane thickness. The hysteresis can be suppressed down to a maximum residual of 0.5 dpt.

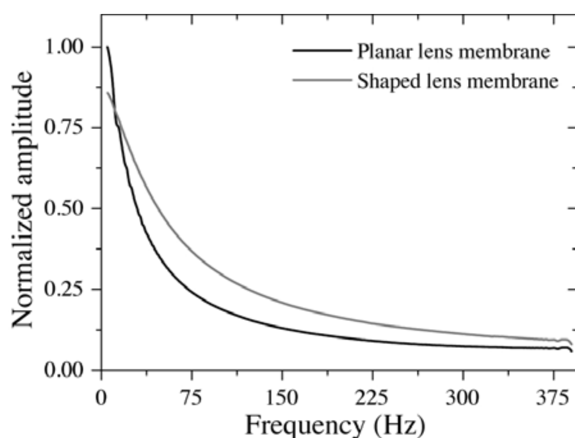

Figure 14: Measured frequency response for a system with a planar (t_{membr} = 60 µm) and a shaped (t_{resid} = 75 µm, R_{mold} = 9.3 mm) lens membrane.

For the dynamical characterization we measure the frequency response (see figure 14) and the full scale response time. The system with a shaped lens membrane shows a more direct response characteristic than a system with a planar membrane, due to the lower membrane amplitude. The full scale response time is measured at a voltage step from +40 to -40 V and reverse. The system with a planar membrane indicates an isotropic response time of 23.9 ms and the lens with a shaped membrane a time of 35.4 ms. This arises from the higher lens back pressure of the inhomogeneous membrane, which let the response time increase.

4. CONCLUSIONS

The use of adaptive lens systems with homogeneous, respectively, inhomogeneous membranes is application specific. On the one hand, systems with planar membranes are reasonable for a large focal length range, a constant optical lens quality and a short response time. On the other hand, the application of lenses with shaped membranes is reasonable for a higher optical lens quality at a smaller focal length range around a working point.

5. REFERENCES

[1] B. Berge and J. Peseux: "Variable focal lens controlled by an external voltage: an application of electrowetting," *Eur. Phys. J. E,* Vol. 3, pp. 159-163 2000.

[2] Optotune: "Electrical focus tunable lens EL-6-22," *Datasheet*, 2008.

[3] H. Ren, D. Fox, P. A. Anderson, B. Wu and S.-T. Wu: "Tunable-focus liquid lens controlled using a servo motor," *Opt. Express*, Vol. 14, pp. 8031-8036, 2006.

4] F. Schneider, C. Müller and U. Wallrabe: "A low cost adaptive silicone membrane lens," *J. Opt. A: Pure Appl. Opt.,* Vol. 10, 044002, 2008.

[5] F. Schneider, J. Draheim, C. Müller and U. Wallrabe: "Optimization of an adaptive PDMS-membrane lens with an integrated actuator," *Sens. Actuators A: Phys.*, doi:10.1016/j.sna.2008.07.006, 2008.

[6] F. Schneider, J. Draheim, R. Kamberger and U. Wallrabe: "Process and material properties of polydimethysiloxane (PDMS) for Optical MEMS," *Sens. Actuators A: Phys.*, Vol. 151, pp. 95-99, 2009.

[7] S. Reichelt and H. Zappe: "Combined Twyman–Green and Mach–Zehnder interferometer for microlens testing," *Appl. Opt.*, Vol. 44, pp. 5786-5792 (2005).

FEASIBILITY OF OPTICAL CLOCK DISTRIBUTION FOR FUTURE CMOS TECHNOLOGY NODES

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Abstract: CMOS is arguably the most successful semiconductor technology in electronics history. This is clear by the constant efforts involved in scaling as the key driver of improving the performance of ICs to keep up with consumer expectations. However, this trend has lately been haltered by another on-chip component: the interconnect. As scaling decreases active device dimensions for a corresponding performance increase, interconnect dimensions suffer under reduction due to increasing capacitance and resistance. One possible solution might be to move the long, power consuming global signal nets into the optical domain. This paper compares predicted electrical versus optical global signal distribution for future nanometre CMOS nodes, based on clock distribution and the associated power consumption.

Keywords: Optical interconnect, CMOS, optical clock distribution, hybrid.

1. INTRODUCTION

CMOS still has an immense impact as the dominant semiconductor technology for mass integration. Given the monetary and development investment up to date, the industry is throwing its full weight behind the continuation of scaling, both in terms of function density and in performance. With various breakthroughs on device level, the limitations on future scaling lie in the development of adequate interconnects to support the increase in logic density. There are numerous factors influencing the interconnect architecture used. None more so than the global clock distribution scheme. In modern microprocessor units (MPUs), the clock distribution network can be the single most power consuming entity.
This work aims to take the International Technology Roadmap for Semiconductors (ITRS) [1] requirements for future technology nodes, along with predictive SPICE modelling, in order to extrapolate on what can be expected from future electrical clock networks. As a comparative platform, an electrical H-tree is characterised in terms of its electrical power consumption components. The results are then used to indicate the feasibility of optical clock networks as device dimensions decrease.

2. PREDICTIVE TECHNOLOGY MODEL

In order to produce sensible circuit performance results, predictive SPICE modelling is used. Based on models developed by [2] and updated with the latest ITRS [1] predicted requirements for devices, SPICE based models are employed for the simulation of the optical front end receiver and clock buffer circuits. This method ensures that aspects such as short circuit currents on switching events and device drain capacitances, which may influence the results substantially, are incorporated into the prediction.

3. COMPARATIVE ARCHITECTURE

3.1 An overview of future technology parameters

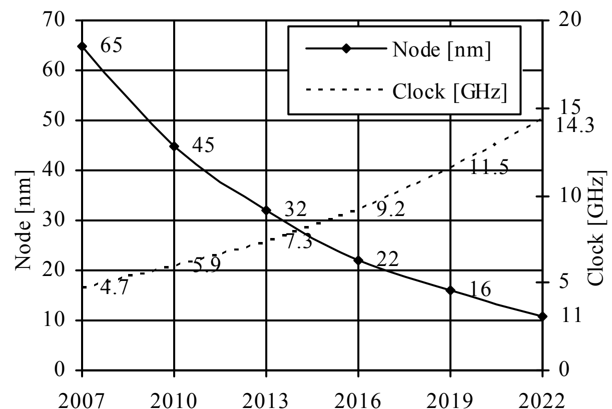

Figure 1: CMOS scaling and local clock frequency timeline.

The ITRS publishes data on an annual basis wherein technology requirements are stipulated, based on past technology trends and future market interests. Combining this information with physical modelling of, for instance, the interconnects and CMOS active devices, key technology parameters affecting the performance of clock networks can be derived. Figure 1 shows the predicted trend for CMOS scaling within the next decade, along with the expected local clock frequencies. Table II summarises the most important characteristics that can be derived from process predictions, to be expected in the near future. Logic area is predicted to maintain a relatively constant portion of chip area, as opposed to the great reduction of logic portion in [3], since both logic and SRAM functions are expected to increase at the same rate [1]. Intel's 45nm Penryn [3] reinforces this trend

Table I: Overall technology characteristics.

Parameters	Units	65nm	45nm	32nm	22nm	16nm	11nm
System characteristics							
V_{DD}	[V]	1.1	1.1	1	0.9	0.9	0.8
f_{clk}	[GHz]	4.7	5.9	7.3	9.2	11.5	14.3
Logic area	[cm^2]	2.86	2.87	2.87	2.88	2.88	2.88
D_{xtor}	[M/cm^2]	357	714	1427	2854	5708	11416
Device characteristics							
I_{on}	[µA/µm]	1006	1370	1948	1943	2344	2533
$L_{physical}$	[nm]	32	24	18	14	10.7	8.1
T_{oxp}	[nm]	1.2	0.95	0.7	0.7	0.6	0.55
T_{oxe}	[nm]	1.85	1.27	1.1	1.1	1	0.95
V_{th}	[mV]	225	175	103	105	109	109
Global interconnect characteristics							
r_{int}	[Ω/µm]	0.39	0.91	1.74	3.53	6.20	12.67
c_{int}	[F/µm]	2E-16	1.8E-16	1.7E-16	1.5E-16	1.5E-16	1.3E-16
Local interconnect characteristics							
r_{int}	[Ω/µm]	1.20	2.74	5.14	10.33	19.53	39.35
c_{int}	[F/µm]	1.8E-16	1.6E-16	1.5E-16	1.3E-16	1.3E-16	1.1E-16

where the logic area portion remained roughly the same as the previous generation MPU, although the core size is smaller than predicted for high performance MPUs [1]. The current trend is roughly double the functions per area from one technology generation to the next. On a device level, where channel depths become small enough, it is important to include the quantisation effects as an electrical equivalent oxide thickness. The physical thickness represents the effective thickness for SiO_2, while newer high-κ solutions might utilise thicker gates to minimise gate tunnelling [4]. I_{on} shows the strong inversion saturation current for NMOS devices at logic levels. The interconnect resistance and capacitance terms were calculated assuming full shielding, with minimum dimensions used for maximum density. Resistivity calculations consider effective resistance increases as dimensions decrease, including the grain boundary component, as well as the inclusion of the skin effect at high frequencies.

3.2 Clock tree topology

The three most often used topologies include grids, trees and length matched serpentines [5]. Given the capacitive and skew advantages of tree structures, the symmetrical H-tree is used as a comparative topology for comparing electrical and optical power consumption performance. This topology applies to the distribution of the global clock signal, where handover occurs at the end points into local clock regions constructed with a local grid. This local region is fed by a local clock buffer and will be common to both electrical and optical networks. Each end point sees exactly the same path as any other from the source, making skew depend only on process and environmental variations. For the purpose of this work, a square die is assumed, sized according to the predicted logic portion of a typical modern MPU. Figure 2 shows a die partitioning using an H-tree, with n representing the tree depth. Note that n for this work is not necessarily defined the same as compared to other works [3], [6]. For each increment of n, four new terminations, or end points will be instanced per (n - 1) level end point. A summary of characteristics in a typical H-tree network is shown in Table II. The depth of the tree, n, is determined by the

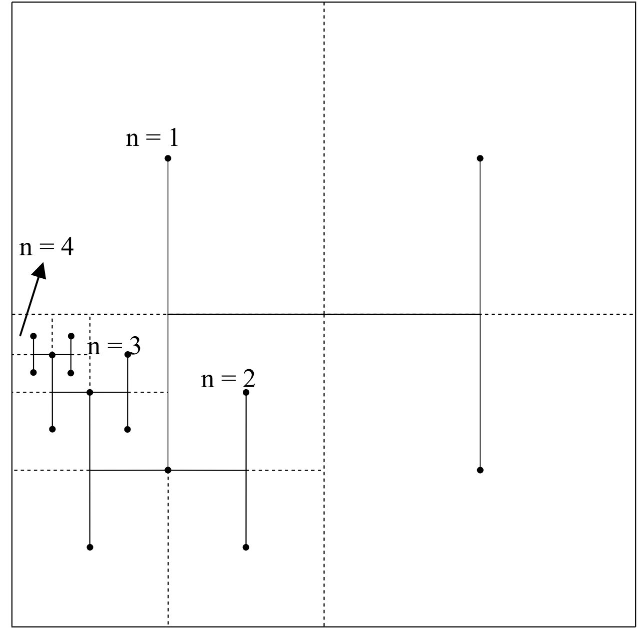

Figure 2: Partitioning of an H-tree.

maximum allowable skew for a local region, defined in [3]. As technology scales and the skew reaches a certain critical limit, the depth is incremented. The introduction of repeaters between tree splits along the segment becomes important to maintain signal flanks of an acceptable level. The 20 % - 80 % transition time metric is used, where this should be maintained below 10% of the relevant technology node's clock period, T_{clk}. The expressions developed in [7] can be modified to determine an expression for the interconnect length at which the transition time does not meet the stated criteria (see Section 4.1).

3.3 Tree depth and local region design

The depth of the tree is determined by the maximum allowable skew within a local region; that is, after a global end point feeds the local clock grid. Given the known transistor density, it is assumed for the purpose of calculations that a there are 64 gates in a register and 25 transistors per gate. If the local region dimensions are known, it is possible to calculate the number of registers in a local region and consequently determine the longest Manhattan-type interconnect length from the local region

Table II: H-tree length equations.

Equation	Description
$\frac{3}{4}L\sum_{k=1}^{n}2^k$	Total H-tree length
$3\times L\times 2^{n-2}$	Length contributed at level n
$L\times 2^{-(n+1)}$	Segment length at level n
$3\times 2^{2n-1}$	Number of segments at level n
$L^2/2^n$	Area of local region at level n
$l_{die}/2^n$	Local area sidewall dimension
2^{2n}	Number terminating end points

buffer to the farthest register. This then represents the path of worst skew within a local region. If a maximum skew of 10 % of the clock period is used, it is possible to determine how deep the tree needs to be to adhere to the local skew requirements.

Table III: Tree and repeater design for future nodes.

Parameters		65nm	45nm	32nm	22nm	16nm	11nm
Tree design							
Max local l_{seg}		464.2	296.4	201.9	138.0	90.3	62.2
Tree depth n		6	6	7	7	8	9
# of end points		4096	4096	16384	16384	65536	262144
Max global l_{seg}		412.73	260.93	193.62	126.23	84.17	56.03
# of repeaters		4850	7070	19532	28484	80642	311798
# of split buffers		6142	6142	24574	24574	98302	393214
Repeater design parameters							
A	[Ω·µm]	695.8	575.65	395.4	366.15	315.65	273.25
B	[F/µm]	5.7E-15	4.8E-15	2.9E-15	3.0E-15	3.0E-15	2.9E-15
R		0.35	0.37	0.47	0.44	0.43	0.42
W	[µm]	13.36	7.98	5.35	3.46	2.45	1.51

4. CIRCUIT DESIGN

4.1 Electrical repeater circuits

$$\begin{aligned} a &= 0.5545 r_{int} c_{int} \\ b &= 1.386\left(r_{int} C_B + c_{int} R_B\right) \\ c &= 1.386 R_B C_B - T_{10\%} \\ l_{seg} &\leq \frac{-b+\sqrt{b^2-4ac}}{2a} \end{aligned} \tag{1}$$

Equation 1 shows the maximum allowable interconnect length before the 20 % - 80 % time degrades beyond $T_{CLK}/10$. The repeaters are sized to minimise l_{seg}. A limit of two inverter pairs per repeater is set to maintain practicality. The input inverter pair is sized smaller compared to the output pair by a ratio R. This has the advantage of reducing the input capacitance, while maintaining a stronger driving capability. A lower limit exists on the value of R to maintain the requirement of a 20% - 80% transition time between inverter pairs. Equation 2 quantifies the lower limit based on the timing constraints.

$$R = \frac{1.386AB}{T_{10\%}} \times 1.1 \tag{2}$$

$T_{10\%}$ is one tenth of a clock period and the factor of 1.1 is inserted as a safety margin to ensure that the inter-stage transition time is not limiting. Although Equation 2 states a limit, an optimal value for R can be found if the total capacitance, that is the sum of the interconnect and repeater components, are normalised to a per unit length metric.

$$\frac{\partial C_{total/length}}{\partial R} = \frac{\partial}{\partial R}\left(c_{int} + \frac{B \times W \times (1+R)}{l_{seg}}\right) = 0 \tag{3}$$

Solving Equation 3, with l_{seg} as the maximum allowable segment length and c_{int} as the interconnect capacitance per unit length, yields a solution for an optimal R value. The optimal width W represents a scaling factor for transistor width, where A and B represent width dependent input capacitance and output resistance parameters of the buffer determined through maximising the segment length in Equation 1, shown in Equation 4.

$$W = \sqrt{\frac{c_{int} A}{r_{int} RB}} \tag{4}$$

4.2 Photodiode design

One limiting factor in the design of an optical system is that the photodiode does not scale along with technology. This is partly due to the lower limit on the physical dimension of the *pn*-junction region to accommodate the wavelength of incident light. Another important factor is the light intensity per unit area, which becomes unrealistic if the photodiode active region is too small. Based on [8] it is possible to obtain multi-gigahertz operation with an *n*-well based photodiode with a responsivity of 0.3 A/W, with a device capacitance of 5 fF.

4.3 Optical receiver

The chosen topology for the optical receiver front end is a high impedance design, similar to the approach in [3]. Figure 3 shows the configuration, where the photodiode discharges the input node in order to generate a logic transition by the first inverter. The following cascade of inverters serves both to delay the transition and to buffer the signal for subsequent stages. The signal v_{CH} then recharges the input node after the cascade dependent delay.

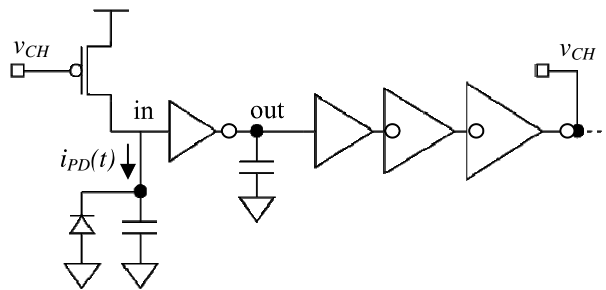

Figure 3: High impedance switched optical front end.

Although this requires a relatively strong optical pulse, the duration thereof may be very short. This topology is also well suited to standard cell compatibility, has a far superior noise performance when compared to transimpedance amplifier (TIA) approaches, and only consumes power on transitions. Most of the power consumed is due to the inverters required for driving a local region clock buffer.

5. POWER CONSUMPTION

5.1 SPICE simulations

It is possible to, from a completely theoretical perspective, utilise the following equation to determine the dynamic power dissipation of the clock networks (Equation 5).

$$P_{dyn} = C \times f_{clk} \times V_{DD}^2 \quad (5)$$

The true power consumption will increase due to short circuit currents on a switching event, and buffer output capacitances, which are difficult to model by hand. Therefore, predictive models (see Section 2) are used to estimate a more accurate quantity for expected power consumption of circuits and interconnects, which is used in the subsequent comparisons. This will obviously be more comprehensive than simply using Equation 5.

5.2 Electrical components

Figure 4 shows the resulting power consumption based on the above methodology. Because the interconnect dimensions is kept at minimum, the power consumption of the supporting circuitry for maintaining signal fidelity, namely the repeaters, are responsible for a substantial contribution to the overall power consumption. Of course, increasing the interconnect dimensions results in the component power being replaced by an increased interconnect component. It is also clear that the deep tree in the 16 nm and 11 nm nodes are contributory to the sharp increase in global power consumed.

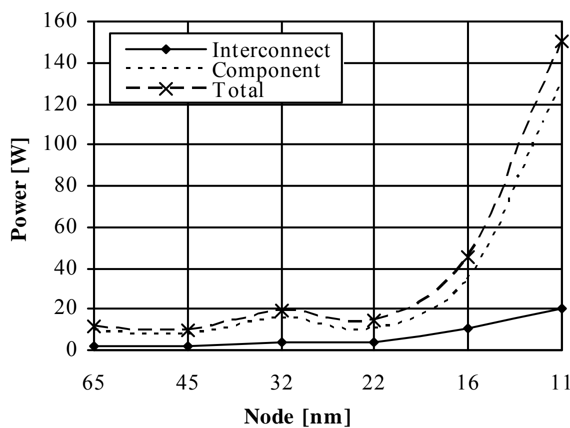

Figure 4: Electrical network power consumption.

5.3 Optical components

Figure 5 shows the situation when a fully optical tree replaces the electrical tree in Section 5.2. It becomes clear that the optical power required to maintain reasonable operation also suffers at the smaller nodes. One big reason for the sudden increase is the constant charging capacitance present on the input node in Figure 3, while the operating frequency increases. This is due to the large photodiode capacitance, which is assumed to remain constant throughout. The electrical component represents the power required to amplify the signal enough to drive a local region buffer, as well as recharging the input node capacitance back to a high logic state.

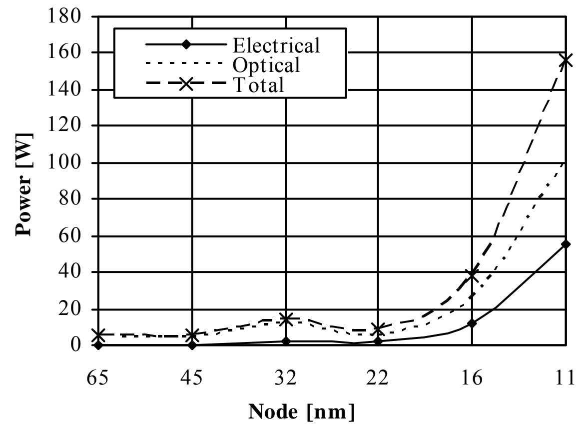

Figure 5: Optical network power consumption.

5.4 Hybrid network performance

From Figure 4 and Figure 5 it is clear that the 16 nm and 11 nm nodes presents a limit to where optical networks will outperform electrical networks. Figure 6 shows the total global clock network power consumed when the tree is made up of an optical tree up to level *n*, and then continues as an electrical tree for the rest of the tree levels. It is interesting to note that an optical tree stopping at level 7 is just as power hungry as a fully optical tree (stopping at level 8), while the required external power efficiency (EPE) to beat a completely electrical network is less stringent. Note that this EPE value does not include propagation, bending and coupling losses.

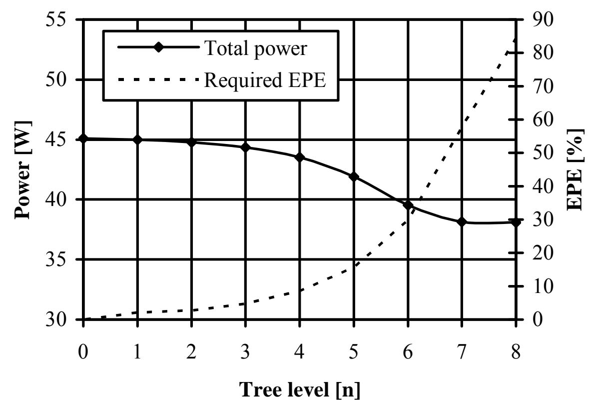

Figure 6: Total power with optical tree up to different depths, 16 nm node.

An even more interesting result is shown in Figure 7, where it can be seen that the total power consumption of the clock network decreases as the optical tree is introduced at deeper levels, but only up to a point. After a tree depth of 7 the overall power consumption increases drastically, where the required EPE to beat an electrical

system exceeds 100 %, showing that the optical network fails to surpass the performance of an electrical one.

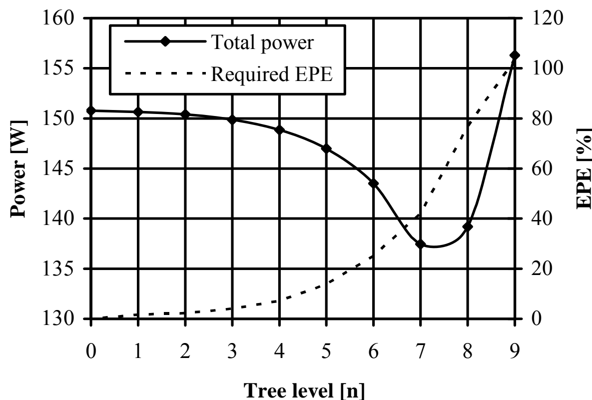

Figure 7: Total power with optical tree up to different depths, 11 nm node.

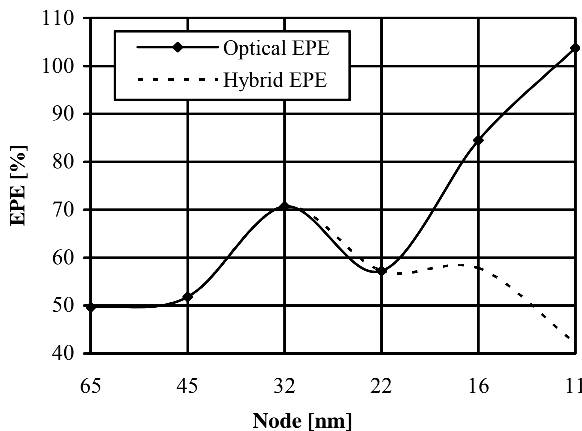

Figure 8: Optical vs. hybrid network EPE.

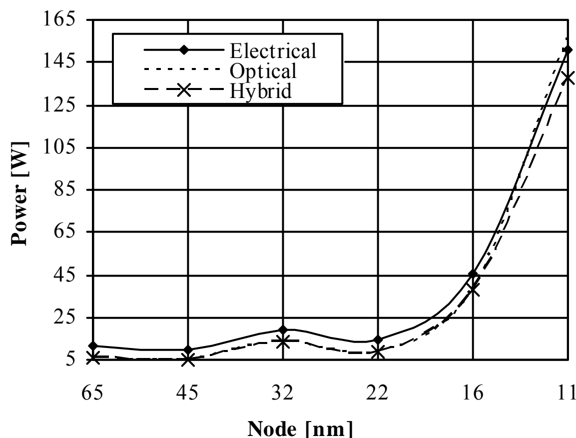

Figure 9: Electrical, optical and hybrid network total power consumed.

This shows that the optimal power consumption might be obtainable if a hybrid network is considered. Figure 8 shows that a hybrid network also relaxes the requirement for the source EPE, allowing more headroom for losses. Figure 9 shows the resulting power consumption comparisons for fully electrical, fully optical and hybrid networks for the 65 nm to 11 nm nodes.

6. CONCLUSION

The future of interconnect technology, especially for global signals, might not necessarily find solutions in a completely pure move from electrical to optical, but rather in exploiting the advantages of both in the form of hybrid networks. It is also seen that there are some fundamental limits to scaling down the optics before it would really contend as a replacement for electrical networks. For now, if light sources and on chip interconnects can handle the requirements, it would seem that optical networks are already viable for replacing electrical networks at a global signal level.

7. REFERENCES

[1] ITRS 2008 Updated Report. [Online]. Available: http://www.itrs.net

[2] W. Zhao and Y. Cao, "A new generation of predictive technology model for sub-45nm design exploration," in *Proc. of the 7th International Symposium on Quality Electronic Design*. 2006, pp. 585-590.

[3] B. Ackland, B. Razavi, and L. West. "A comparison of electrical and optical networks in nanometer technologies," In *Proc. of the IEEE 2005 Custom Integrated Circuits Conference*, pages 779-782.

[4] G. Varghese *et al*. "Penryn: 45-nm next generation Intel® core™ 2 processor," In *Proc. of the Asian Solid-State Circuits Conference*, 2007, pages 14-17

[5] P. Restle and A Deutsch, "Designing the best clock distribution network," in *IEEE Symposium on VLSI Circuits*, Honolulu, HI, USA, Jun 1998, pp. 2-5.

[6] E. Friedman. "Clock distribution networks in synchronous digital integrated circuits," *Proceedings of the IEEE*, 89(5):665-692, May 2001.

[7] T. Sakurai. "Closed-form expressions for interconnection delay, coupling, and crosstalk in VLSIs," *IEEE Trans. on Electron Devices*, 40(1):118-124, Jan 1993.

[8] S. Radovanovi´ , A.-J. Annema, and B. Nauta, *High-speed photodiodes in standard CMOS technology*. Springer, 2006.

SURFACE PASSIVATION APPLICABLE TO InAsSb/GaSb PHOTODIODES FOR INFRARED DETECTION

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Abstract: In this paper the influence of various anodisation solutions on the surface passivation of InAsSb/GaSb photodiodes is examined. The diode structure is based on a design reported by Bubulac et al. [1]. The diode consists of a p-i-n structure grown by MOCVD and nearly lattice matched to a GaSb substrate. The structure, p-$InAs_{1-x}Sb_x$/n-$InAs_{1-x}Sb_x$/n-GaSb (x = 0.10 in both cases), consisted of a Zn-doped p-type layer and an unintentionally doped n-type layer on the n-type substrate. To define the active area of the photodiode, mesas were etched with a sulphuric acid based solution. Three anodisation solutions, containing Na_2S, KOH or $(NH_4)_2S$, were tested. Four sets of diodes were processed, using each of the three anodisation solutions as well as an unpassivated reference detector. The effect of passivation was studied by current-voltage measurements, yielding the reverse bias current, as well as by responsivity measurements.

Key words: Photodiode, surface passivation, anodisation, MOCVD, p-i-n structure, InAsSb.

1. INTRODUCTION

Given all the advantages offered by InAsSb several researchers have explored the possibilities of creating devices based on this compound. The greatest advantage of a ternary compound is the versatility that it allows one in engineering the size of the energy band gap. In the case of $InAs_{1-x}Sb_x$ the mole fraction of antimony in the compound can potentially vary the cut-off wavelength between 3.1 υm and 9.0 μm at 77 K, a spectral range hitherto dominated by the HgCdTe compound. InAsSb presents an improvement on some of the physical disadvantages given by HgCdTe. HgCdTe tends to be quite brittle, making handling and processing very difficult. This is caused by the large atomic numbers creating weak bonds with a large ionic component. The III-V family, to which the InAsSb compound belongs, possesses lower atomic numbers, causing stronger bonds of a more covalent nature. Another drawback of HgCdTe is that Hg diffuses at temperatures around 300 K. InAsSb can withstand processing steps at higher temperatures. From a material growth perspective the steep gradient of the HgCdTe band gap against Cd mole fraction relation presents a major challenge. The HgCdTe band gap has a much stronger dependence on the Cd mole fraction than the InAsSb band gap has on the Sb mole fraction. The practical implication is that the cut-off wavelength of detectors on a single HgCdTe wafer may differ from one surface area to the other - creating difficulties especially with detector matrix applications.

One of the greatest obstacles to overcome has been the lack of a suitable substrate for the production of high quality epitaxial layers. It is well-known that misfit dislocations, arising from lattice-mismatch between epitaxial structures and the substrate will cause defects, giving rise to trap assisted tunnelling, which in turn introduces a strong 1/f noise factor to the detector current [2] and severely limits the R_0A factor. The zero bias resistance of the detector, R_0, is the derivative of the I-V (current-versus-voltage) curve at zero bias voltage, this is influenced by both the material resistance and the size of the active area of the diode. The R_0A product, where A is the active area of the diode, is a figure of merit used to compare diodes with different active areas. Diodes with larger active areas tend to have smaller R_0 values.

Epitaxial growth of InAsSb on several substrates has been explored including GaSb [1, 3-6], GaAs [3, 7-11], and InAs [12-14]. Growth on GaAs or Si [15, 16] is a very attractive option because of the advantages it offers for the development of large area focal plane arrays and for the monolithic integration of the detector array with the readout circuit. Very high quality GaAs and Si substrates are readily available in large sizes. Even though Si technology is more established and extremely popular, it is possible to manufacture readout circuits on either Si or GaAs.

Rogalski et al. [17] explored the idea of growing $InAs_{1-x}Sb_x$ epitaxial layers on $Ga_{1-x}In_xSb$ substrates, which allows tuning of the lattice constant as well as the band gap of the substrate to complement that of the active layer.

Several workers have researched the qualities of InAsSb heterojunctions grown on GaSb substrates [3, 8, 10]. Srivastava et al. [3] have reported I-V and C-V measurements on n-$InAs_{0.95}Sb_{0.05}$/n-GaSb structures and found the n-n heterojunction to be strongly rectifying and behaving like a metal/n-GaSb Schottky diode with a barrier height of 0.8 ± 0.002 eV. They have established

that the band line up is of the broken gap variety. They have measured the valence band offset E_V(GaSb) - E_V(InAsSb) to be 0.67 ± 0.04 eV and concluded that the electrical characteristics of n-$InAs_{0.95}Sb_{0.05}$/n-GaSb heterojunctions are controlled by large band bending on the GaSb side of the junction.

Giani et al. [10] have done room temperature I-V measurements on lattice-matched n-$InAs_{0.91}Sb_{0.09}$/n-GaSb and p-$InAs_{0.91}Sb_{0.09}$/n-GaSb junctions. They also found the n/n heterostructure to be rectifying with a dark current of 70 µA at 1 V reverse bias. The p/n junction, on the other hand, was reported to be ohmic. This group measured the photoconductivity spectra of their n/n device at 300 K as well as at 77 K and found the response at 77 K to be nine times higher. They attributed this partly to an increase in the carrier lifetime.

Rakovska et al. [5] states that the GaSb/$InAs_{1-x}Sb_x$ interface is known to be semi-metallic, leading to massive flooding of the $InAs_{1-x}Sb_x$ layer by electrons from the valence band of the GaSb. In order to reduce the carrier population at the interface, they introduced a 30 nm $Al_{0.47}Ga_{0.53}Sb$ layer followed by an 18 nm $In_{0.85}Al_{0.15}As_{0.9}Sb_{0.1}$ layer to act as a barrier between the $InAs_{1-x}Sb_x$ layer and the GaSb. This resulted in narrower photoluminescence peaks and less noisy conductivity spectra.

Podlecki et al. [9] reported two types of noise behaviour for their MOCVD grown $InAs_{0.91}As_{0.09}$/GaAs diode structure. At low frequencies they observed a dominating 1/f noise that they attributed to non-optimised contacts. At higher frequencies they inferred noise due to generation-recombination processes.

In this paper the influence of the various surface passivation recipes tried in this study on the reverse bias dark current is examined for a photodiode based on a design reported by Bubulac et al. [1]. This group reported results on a p-i-n structure grown by LPE and nearly lattice matched to a GaSb substrate. The structure, p-$InAs_{1-x}Sb_x$ /n-$InAs_{1-x}Sb_x$/ n-GaSb (x = 0.10 in both cases), consisted of a Zn-doped p-type layer and an unintentionally doped n-type layer on the n-type substrate. In both cases the carrier density was reported to be 10^{16} cm^{-3}.

They observed a short wavelength cut on of 1.4 µm at 77 K, which is determined by the band gap of the GaSb substrate. The cut off wavelength was determined by the band gap of the n-InAsSb active region, which is composition dependent. They reported a 50 % cut off wavelength of 4 µm for devices with an antimony mole fraction of 0.10. AgMn was evaporated to establish ohmic contact to the front of the device and the backside contact was established by bonding the device with silver epoxy to a header; this also determined the aperture for backside illumination.

Bubulac et al. [1] determined the electron diffusion length to be almost 27 µm at 100 K and the hole diffusion length to be 5.5 µm. The hole diffusion length in GaSb was lower than in InAsSb. They established the GaSb reflection coefficient to be about 25 %. In their design they have placed the p-n junction 3 µm from the metallurgical interface with the substrate, i.e. less than the hole diffusion length, because shorter wavelength photons would be absorbed very close to the hetero-interface and holes would have to diffuse further to reach the junction. They measured the total InAsSb thickness to be 10 µm thick.

The photo-response of their detector covered a spectral range of 1.7 to 4.2 µm, achieving an external quantum efficiency of 65 % without anti-reflection coating. At 100 mV reverse bias, the diode current was measured to be less than 10^{-9} Acm^{-2}, with an R_0A product of 10^9 Ωcm^2.

2. EXPERIMENTAL METHODS

2.1 Device processing

The structure that was processed and evaluated in this work was based on the design by Bubulac et al. [1]. A p-i-n structure consisting of p-$InAs_{0.91}Sb_{0.09}$/n-$InAs_{0.91}Sb_{0.09}$/n-GaSb were grown by MOCVD, commissioned from Spire Bandwidth Semiconductor, LLC, situated in Hudson (New Hampshire, U.S.A). The (111)A GaSb substrate (487 µm thick) is Te doped to a carrier concentration of 2 x 10^{17} cm^{-3}. The p-$InAs_{0.91}Sb_{0.09}$ layer (7 µm thick) is Zn doped to a carrier concentration of 2 x 10^{18} cm^{-3} and the n-$InAs_{0.91}Sb_{0.09}$ layer (3 µm thick) not intentionally doped to a carrier concentration of 3 x 10^{16} cm^{-3}. The objective of this experiment was to investigate the effects of an anodic layer with respect to surface passivation. Previously [20] the success of the strategy was tested with the use of C-V measurements on MIS (Metal-Insulator-Semiconductor) devices. In this work the success of the passivation strategy will be evaluated through the resulting influence on the dark current and responsivity of an infrared photodetector.

A mesa pattern (diameter 4 mm)was first deposited by standard photolithographic procedures and etched to a depth of 8 µm. A sulphuric acid based etchant (H_2SO_4 (95-97 %) : H_2O_2 (30%) : H_2O, 50 ml : 1 ml : 100 ml) was used at 30 ˚C for 24 minutes, resulting in a mesa height varying from 7.5 µm to 8.8 µm. Next, an anodic layer was grown in order to passivate the etched surface. In addition to the three anodic solutions (KOH, Na_2S and $(NH_4)_2S$) one sample was left unpassivated to act as a reference. Finally a 6000 Å SiO_2 layer was deposited by UV enhanced CVD (ultraviolet enhanced chemical vapour deposition) to act as an anti-reflection layer before metal contacts were thermally evaporated. The metal contacts consisted of 60 nm Ti followed by 1.2 µm Au. In addition to achieving electrical contact, the metal layer

also served to define the front illuminated optical area with a 4 mm diameter.

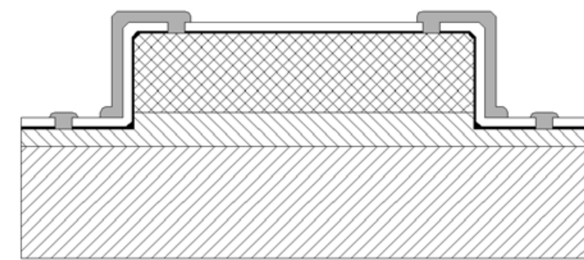

Figure 1: The InAsSb diode structure.

2.2 Current-versus-voltage measurements

All I-V measurements were done under dark room conditions. The I-V characteristics were measured using an Agilent 1500A parameter analyser. For room temperature measurements the I-V curve was measured from -1.5 V to +1.5 V with the current limited to 3 mA. For measurements at 77 K the output voltage was swept from -1 V to + 1 V with the current limited to 100 µA.

2.3 Electro-optical measurements

The relative responsivity was measured using a Nernst glow source. This source radiates a blackbody spectrum. By placing a monochromator in the optical path, specific wavelengths can be selected. The light from the monochromator was directed unto an optic table which reflected 30 % of the signal to a reference detector and 70 % to the processed InAsSb detector.

The reference detector was a ZnSe pyroelectric detector with a wavelength independent responsivity, in the range 1.2 µm to 14 µm. Due to the wavelength dependence of the monochromator throughput, the signal from the detector under test was normalised against the output from the reference detector.

In order to do absolute responsivity measurements, the diode structures were mounted inside experimental dewars, each with a sapphire window, yielding an average transmission of 80 % within the applicable wavelength region (i.e. 2.3 to 4.8 µm). The dewars were evacuated to a pressure below 2 x 10^{-2} mbar. The 20 % signal loss was compensated for in the calculations of the responsivity values.

The detector was set to view a 1000 K blackbody source. A chopper blade in the optical path modulated the signal at 2 kHz. The detector output was amplified by a low noise transimpedance amplifier with a gain of 1 MΩ and measured with an HP3561A dynamic signal analyser. To perform noise measurements the detector was positioned to view a blackbody at room temperature, with an emissivity of greater than 0.9.

3. EXPERIMENTAL RESULTS

Infrared photodiodes were processed on $InAs_{0.91}Sb_{0.09}$ as described in section 2.1. Four sets of diodes were processed, using each of the three anodisation procedures as well as an unpassivated reference detector. The relative responsivity measurements are shown in figure 2. Measurements were done on the untreated sample as well as the Na_2S treated sample, yielding identical results. The measured relative response results correspond very well to that of Remennyi et al. [14]. The detector spectral response yielded a short wavelength 50 % cut on at 3.3 µm and a long wavelength 50 % cut off at 4.3 µm.

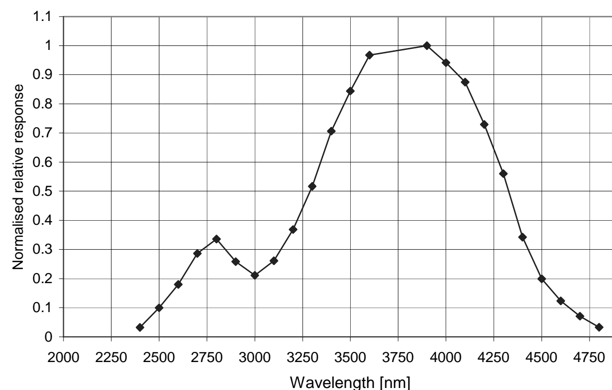

Figure 2: Measured relative response.

Current-versus-voltage (I-V) curves were measured on the four devices in order to investigate the influence of the various surface passivation techniques on the reverse bias dark current of the detectors.

The I-V curves measured on the $InAs_{0.91}Sb_{0.09}$ diodes, measured at room temperature in darkroom conditions, are displayed in figure 3. It can be seen that at room temperature the devices are rectifying.

The turn-on voltage (forward bias) of the diode is shown to be very sensitive to the anodizing solution used. This could be the quality of the anodization layer influencing the surface resistance and thus having an effect on surface leakage currents.

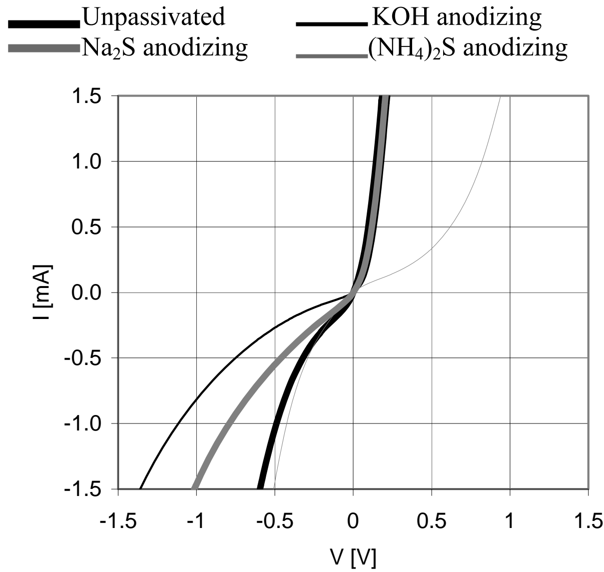

Figure 3: Current vs. voltage characteristics measured at 300 K.

Specific parameters extracted from the I-V curves measured at room temperature for the various surface passivation treatments, are presented in table 1. The parameters measured on a device that had no surface passivation treatment are shown as a reference. It is evident that at room temperature the best zero bias resistance (1270 Ω) was achieved for the sample anodised in KOH. For this device, the lowest zero and reverse bias dark current values are also obtained. Up to a reverse bias of 190 mV all three anodisation treatments seem to reduce the dark current values. For larger reverse bias voltages the $(NH_4)_2S$ passivation yields a dark current slightly larger than that of the reference sample.

Table 1: Device parameters extracted from current vs. voltage measurements at 300 K. Detector current measured at zero bias voltage, I_0, the detector current measured at 0.20 V, $I_{-0.200mV}$ and the detector current measured at 0.40V reverse bias voltage, $I_{-0.400mV}$, are shown.

Passivation	R_{series} [Ω]	R_{0V} [Ω]	I_{0V} [nA]	I_{-200mV} [μA]	I_{-400mV} [μA]
None	72	350	115.0	292.0	694.0
KOH anodising	74	1270	42.1	92.3	199.0
Na_2S anodising	98	824	95.1	165.0	456.0
$(NH_4)_2S$ anodising	202	1000	55.9	297.0	882.0

The dark I-V curves measured on the $InAs_{0.91}Sb_{0.09}$ diodes at 77 K, are shown in figure 4. Again rectifying behaviour is observed and the reverse bias dark current of the detectors are significantly smaller than at room temperature, due to a reduction in thermally generated carriers.

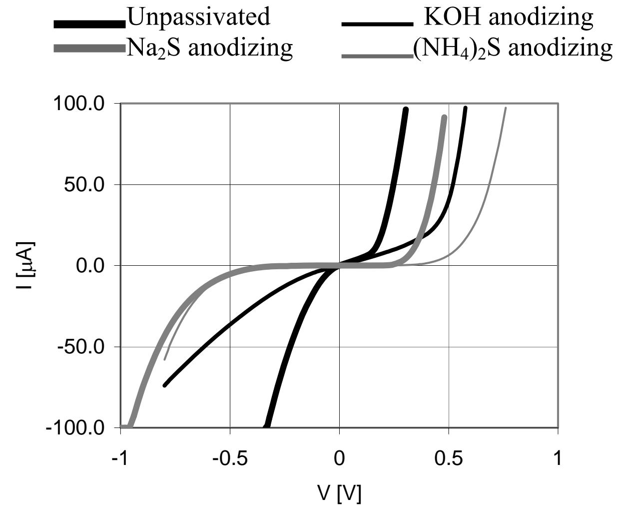

Figure 4: Current vs. voltage characteristics measured at 77 K.

Specific parameters extracted from the I-V curves measured at 77 K, after various surface passivation treatments, are summarised in table 2. At 77 K the highest zero bias resistance (28.5 MΩ) and the lowest zero bias current (4.7 pA) are achieved for $(NH_4)_2S$ passivation. Only for a reverse bias larger than 500 mV does the Na_2S surface passivation yield a lower detector current. All three anodisation treatments result in reduced dark currents as well as lower differential resistance.

Table 2: Device parameters extracted from current vs. voltage measurements at 77 K. Detector current measured at zero bias voltage, I_0, the detector current measured at 0.20 V, $I_{-0.200mV}$ and the detector current measured at 0.40V reverse bias voltage, $I_{-0.400mV}$, are shown.

Passivation	R_{series} [Ω]	R_{0V} [MΩ]	I_{0V} [nA]	I_{-200mV} [μA]	I_{-400mV} [μA]
None	115	0.02	10.7	40.8	100.0
KOH anodising	148	0.3	3.2	9.2	25.9
Na_2S anodising	134	18.4	0.08	0.1	1.9
$(NH_4)_2S$ anodising	379	28.5	0.005	0.1	1.9

Responsivity, noise and detectivity measurements were performed in order to investigate the influence of the various surface passivation treatments on the electro-optical performance of the devices.

The electro-optical parameters measured at 300 K are summarised in table 3. Performance parameters are compared as a result of the various surface passivation treatments. At room temperature the highest D*

(detectivity) is observed for the Na_2S anodisation (1.0 x 10^9 $cm^2Hz^{0.5}W^{-1}$). For this sample, the lowest noise was also achieved (3.9 x 10^{-12} $AHz^{-0.5}$). The unpassivated sample has the worst noise current and the lowest R_0A value.

Table 3: Influence of surface passivation on the electro-optical performance of the photodiode. Measurements were performed at 300 K.

Passivation	R_0A [Ω cm^2]	I_{noise} [pA $Hz^{-0.5}$]	R [mA/W]	D^*_{BB} [$cm^2Hz^{0.5}W^{-1}$]
None	44	6.3	12.0	7.6 x 10^8
KOH anodising	160	4.8	2.1	1.8 x 10^8
Na_2S anodising	104	3.9	10.0	1.0 x 10^9
$(NH_4)_2S$ anodising	126	5.9	7.1	4.4 x 10^8

The electro-optical parameters measured at 77 K are summarised in table 4. The sample passivated in Na_2S yielded the highest D* value at 1.1 x 10^9 $cm^2Hz^{0.5}W^{-1}$, with a noise current value of 3.7 x 10^{-13} $AHz^{-0.5}$. The lowest noise current (2.4 x 10^{-13} $AHz^{-0.5}$) and the highest R_0A value (3.6 x 10^6 Ωcm^2) were measured for the $(NH_4)_2S$ anodisation. All three anodisation treatments seem to improve the noise current by a factor of ~4 compared to that of the reference sample.

Table 4: Influence of surface passivation on the electro-optical performance of the photodiode. Measurements were performed at 77 K.

Passivation	R_0A [kΩ cm^2]	I_{noise} [pA $Hz^{-0.5}$]	R [mA/W]	D^*_{BB} [$cm^2Hz^{0.5}W^{-1}$]
None	2.3	1.1	2.7	9.6 x 10^8
KOH anodising	39.2	0.3	0.5	5.2 x 10^8
Na_2S anodising	2300	0.4	1.1	1.1 x 10^9
$(NH_4)_2S$ anodising	3600	0.2	0.4	7.7 x 10^8

The fact that the responsivity values are so low is ascribed to the quality of the material. The growth process is still being refined.

4. CONCLUSION

It is clear that the diode structure processed in this work displayed current rectification, resulting in a useful device in order to evaluate the success of the chosen surface passivation treatments. Current rectification was obtained at both room temperature as well as at 77 K.

All three anodisation solutions resulted in an improvement in the zero bias dark current over that of the reference diode structure. The highest 77 K D*-value (1.1 x 10^9 $cm^2Hz^{0.5}W^{-1}$) was achieved for the device anodised in Na_2S .

At 77 K the detector yielded a higher series resistance value, lower reverse bias dark current and higher differential resistance when compared to the values measured at room temperature. The noise current of the anodised samples was reduced by about an order of magnitude. The D* values of the KOH and $(NH_4)_2S$ anodised samples improved by about a factor of 2, while there was very little change in that of the untreated sample and the sample anodised in Na_2S. The noise current of the untreated sample improved only by a factor of 6 when cooled down to 77 K. At room temperature the detectors yielded higher current response values but also higher noise values, thus effectively eliminating the change in detectivity.

The highest detectivity value and the lowest noise current were achieved for the sample that had been treated in Na_2S. Thus Na_2S seems to be most effective in reducing the surface state density, which agrees with the results obtained from C-V measurements previously reported [18].

5. REFERENCES

[1] L. O. Bubulac, A. M. Andrews, E. R. Gertner, and D. T. Cheung: "Backside-illuminated InAsSb/GaSb broadband detectors", Appl. Phys. Lett. 36, pp. 734-736, 1980.

[2] A. Krier, H. H. Gao, and Y. Mao: "A room temperature photovoltaic detector for the mid-infrared (1.8-3.4 μm) wavelength region", Semicond. Sci. Tech. 13, pp. 950-956, 1998.

[3] K. Srivastava, J. L. Zyskind, R. M. Lurm, B. V. Dutt, and J. K. Klingert: "Electrical characteristics of InAsSb/GaSb heterojunctions", Appl. Phys. Lett. 49, pp. 41-43, 1986.

[4] A. Marciniak, R. L. Hengehold, Y. K. Yeo, and G. W. Turner: " Optical characterisation of molecular beam epitaxially grown InAsSb nearly lattice matched to GaSb", J. Appl. Phys. 84, pp. 480-488, 1998.

[5] A. Rakovska, V. Berger, X. Marcadet, B. Vinter, K. Bouzehouane, and D. Kaplan: "Optical characterization and room temperature lifetime measurements of high quality MBE-grown InAsSb on GaSb", Semicond. Sci. Technol. 15, pp. 34-39, 2000.

[6] Y. Mao, and A. Krier: "Liquid phase epitaxial growth and photoluminescence of InAsSb grown on GaSb substrates from antimony solution", J. Cryst. Growth 133, pp. 108-116, 1993.

[7] C. Besikci, S. Ozer, C. van Hoof, L. Zimmermann, J. John, and P. Mercken: " Characteristics of

$InAs_{0.8}Sb_{0.2}$ photodetectors on GaAs substrates ", Semicond. Sci. Tech. 16, pp. 992-996, 2001.

[8] G. Bethea, M. Y. Yen, B. F. Levine, K. K. Choi, and Y. Cho: "Long wavelength $InAs_{1-x}Sb_x$/GaAs detectors prepared by molecular beam epitaxy", Appl. Phys. Lett. 51, pp. 1431-1432. 1987.

[9] J. Podlecki, L. Gouskov, F. Pascal, F. Pascal-Delanoy, and A. Giani: "Photodetection at 3.65 µm in the atmospheric window using $InAs_{0.91}Sb_{0.09}$/GaAs heteroepitaxy", Semicond. Sci. Techn. 11, pp. 1127-1130, 1996.

[10] A. Giani, J. Podlecki, F. Pascal-Delannoy, G. Bougnot, L. Gouskov, and C. Catinaud: "Elaboration and characterization of InAsSb grown on GaSb and GaAs substrates", J. Cryst. Growth 148, pp. 25-30, 1995.

[11] A. Bansal, V. K. Dixit, V. Venkataraman, and H. L. Bhat: "Transport, optical and magnetotransport properties of hetero-epitaxial $InAs_xSb_{1-x}$/GaAs(x<=0.06) and bulk InAsxSb1-x(x<=0.05) crystals: experiment and theoretical analysis", Physica E 20, pp. 272-277, 2004.

[12] A. Krier, X. L. Huang, P. Fenge: "Fabrication and characterization of an $InAs_{0.96}Sb_{0.04}$ photodetector for MIR applications ", IEEE Electr. Device L. 25, pp. 283-285, 2004.

[13] P. Chakrabarti, A. Krier, X. L. Huang, P. Fenge, and R. K. Lal: "Optical and electrical characterisation of an p^+-$InAs_{0.96}Sb_{0.04}$/n^0-$InAs_{0.96}Sb_{0.04}$/n^+-InAs photodetector for mid-infrared application", Microwave and Optoelectronics Conference, 2003. IMOC 2003. Proceedings of the 2003 SBMO/IEEE MTT-S International, pp. 87-92 , 2003.

[14] M. A. Remennyi, N. V. Zotova, S. A. Karandashev, B. A. Matveev, N. M. Stus, and G. N. Talalakin: "Low voltage episide down bonded mid-IR diode optopairs for gas sensing in the 3.3–4.3 µm spectral range", Sensors and actuators B 91, pp. 256-261, 2003.

[15] W. Dobbelaere, J. de Boeck, M. van Hove, K. Deneffe, W. de Readt, R. Mertens, and G. Borghs: "Long wavelength $InAs_{0.2}Sb_{0.8}$ detectors grown on patterned Si substrates by molecular beam epitaxy", Electronics Letters, 26, pp. 259-261, 1990.

[16] T. Niedziela, and R. Ciupa: "Ultimate parameters of $Hg_{1-x}Cd_xTe$ and $InAs_{1-x}Sb_x$ n^+–p photodiodes", Solid State Electro. 45, pp. 41-46, 2001.

[17] A. Rogalski, R. Ciupa, and W. Larkowski: "Near room-temperature InAsSb photodiodes: Theoretical predictions and experimental data", Solid State Electro. 39, pp. 1593-1600, 1996.

[18] V. Odendaal, F. D. Auret and J. R. Botha: "On the processing of InAs and InSb for photodiode applications", Physica Status Solidi (c) 5, pp. 580-582, 2008.

ZnO GROWN BY METAL ORGANIC CHEMICAL VAPOR DEPOSITION: EFFECT OF SUBSTRATE ON OPTICAL AND STRUCTURAL PROPERTIES

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Abstract

This paper reports the effects of the following substrates on the optical, structural and morphological properties of ZnO thin films: Si (100), Si (111), c- and r-sapphire, glass, GaAs and ZnO. The thin films were deposited by low pressure Metal Organic Chemical Vapor Deposition using diethylzinc and tertiary butanol as the zinc and oxygen sources, respectively. X-ray diffraction analysis shows that all the ZnO layers are c-axis orientated. Scanning Electron microscopy reveals similar morphology for all the substrates used, with hexagonal columns having cone shape ends being evident. The photoluminescence spectra are similar, but the various transitions have different relative intensities. It is clear that the different substrates influence neither the orientation of the films, nor the surface morphology, significantly. The photoluminescence hints at larger stacking fault densities in films grown on silicon and glass, however, as evidenced by stronger basal plane stacking fault-related luminescence at ~3.319 eV in the relevant low temperature photoluminescence spectra.

Keywords: ZnO, MOCVD, effect of substrates

1. INTRODUCTION

Zinc oxide has attracted much interest in the last two decades because of its wide direct band gap (3.37 eV) and large exciton binding energy of 60 meV at room temperature (300K) [1]. Most recent research on ZnO has focused on its development as an electronic/optoelectronic material, for the manufacture of devices such as light emitting diodes (LEDs) and laser diodes (LDs) [2], piezoelectric transducers [3], optical wave guides, varistor sensors [4], etc. A large body of theory has been developed for a better understanding of the properties of this unique material. For the realization of exciton-based photonic devices, high-quality films are necessary. This has been achieved successfully by different methods, such as molecular beam epitaxy (MBE) [5], magnetron controlled sputtering [6], pulsed laser deposition (PLD) [7], spray pyrolysis [8], sol gel [9], atomic layer deposition (ALD) [10], and Metalorganic chemical vapor deposition (MOCVD) [11]. Among them, MOCVD has proven capable of producing high quality material. Furthermore, this technique yields a high growth rate, superior growth efficiency and large-area uniformity, while in-situ doping is also possible [12].

Several studies have been reported on ZnO grown on different substrates, mainly sapphire (Al_2O_3) [13], Si [14], GaAs [15], bulk ZnO [16] and glass [17]. Different conclusions were made in terms of the influence of substrate on the properties of ZnO films. For example, Fu *et al.* [14] reported that the nucleation of ZnO on Si is difficult. The effect of diffusion of the constituents of the substrate was studied for ZnO deposited on GaAs. Bang *et al.* [15] suggested that GaAs can provide As atoms which can diffuse into the film and act as p-type dopants. ZnO on c-sapphire has been reported to be monocrystalline, with the ZnO c-axis perpendicular to the substrate surface [13]. Growth of ZnO on sapphire is epitaxial, whereas on most of the other commonly used substrates, like Si and GaAs, the films are textured [18].

In this paper the effect of using different substrates on the optical and structural properties of MOCVD ZnO is reported. There are several publications which address the effect of the substrate on MOCVD-grown ZnO films. These studies have compared mainly different orientations of one type of substrate, e.g. c-, r-, a- and m-plane sapphire [19], different orientations of GaAs ((100) versus (111)) [20] or different faces of ZnO (O-face versus Zn-face) [21]. To our knowledge, a comparison of the influence of most of the commonly used substrates for ZnO epitaxy/deposition, namely GaAs, silicon, sapphire and ZnO and their different orientations, has not been reported for the same MOCVD reactor. Clearly further work is required to establish the optimum type and orientation of substrate for high quality ZnO films.

EXPERIMENTS

MOCVD was used to grow ZnO thin films on different substrates in a separate inlet quartz reactor tube, in

order to avoid pre-reactions between precursors. Diethylzinc (DEZn, $(C_2H_5)_2Zn$) and tert-butanol (TBOH, $(CH_3)_3CHO$) were used as Zn source and O source, respectively. The DEZn molar flow was kept at 17.2 µmol/ min and the DEZn bubbler temperature was kept at 25 °C. The TBOH molar flow rate was 1024.7 µmol/ min and the bubbler was kept at 40°C. High purity (5N) argon gas was used to transport the sources to the reactor. The total flow of argon through the reactor was 1.22 l/min. The growth temperature was 380°C and the pressure in the reactor was maintained at 20 Torr. The growth time was 30 minutes, yielding films with thickness between 2 and 4 µm.

All the substrates were degreased in trichloroethylene (5 min), acetone (5 min) and methanol (5min), then rinsed in de-ionized water and blown dry with nitrogen. The glass, GaAs, ZnO and sapphire substrates were not etched subsequent to degreasing. The silicon surface was etched for one minute in $HF:H_2O$ (1:10) in order to remove the SiO_x, then rinsed in de-ionized water and blown dry with nitrogen. The sapphire and ZnO substrates were annealed at 900°C in an oxygen environment for 1h, which should result in the formation of atomic steps on the substrate surface. Such steps on the annealed substrate are expected to be favorable for ZnO epitaxy [22].

The growth experiments were performed in two growths run. The reactor geometry allowed placement of only four substrates on the graphite susceptor. The first growth run was performed on glass, GaAs and the two orientations of silicon, while deposition on the other four substrates took place in the second growth run.

The crystalline quality of ZnO films was determined by X-ray diffraction using Cu Kα_1 radiation (λ = 0.154056 nm). The surface morphology of the samples was studies using a Philips XL30 scanning electron microscope (SEM). Low temperature photoluminescence was used to study the optical properties of the different samples. The PL was excited with a 325 nm line of a He–Cd laser, while a Hamamatsu R3896 photomultiplier tube was used for detection. A closed-cycle He cryostat was used to cool down the samples.

2. RESULTS AND DISCUSSION

3.1 Structure

Fig. 1 shows the normalised XRD patterns of ZnO thin films on different substrates. Only the (0002) peak of ZnO is observed in each case, showing preferred c-axis orientation of the layers. The dominance of the (0002) ZnO peak for all substrates indicates that the substrate type and orientation do not influence the orientation of the films. Van Drift reported that even in the absence of epitaxy, the preferred film orientation can often be explain by the evolutionary selection rule, which states that the fastest growing crystallographic plane will dominate other planes and thus determine the final orientation [24]. The insert in Fig. 1 shows the full-width at half-maximum (FWHM) of the films. The FWHM has been extracted by doubling the half-width at half-maximum, measured on the low-angle side of the lines. This was done in order to minimize the influence of overlap between the Kα_1 and Kα_2 peaks.

The XRD peak width is inversely proportional to the grain size, according to Scherrer's formula [24]. The average grain sizes obtained from this formula range between 46 nm for GaAs substrate and 78 nm for ZnO (O) substrate.

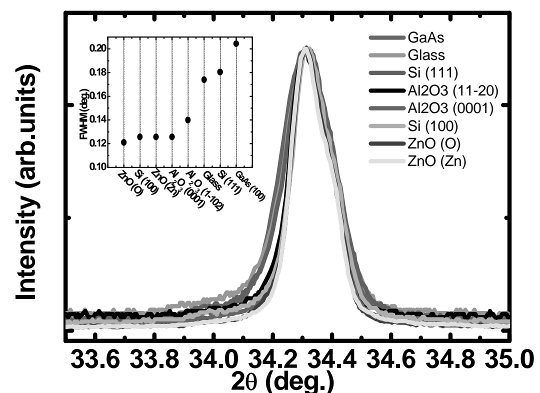

Figure 1: Normalized XDR spectra of ZnO films grown on different substrates.

3.2 Morphological analysis

In Fig. 2 the surfaces of the ZnO films grown on the various substrates are shown. The morphologies are similar, with hexagonal columns having cone shaped ends being evident. In all cases these columns are roughly perpendicular to the substrates, as shown in a cross-sectional SEM view for one of the samples in Fig. 3. The observed columnar growth is a result of the high growth rate along the c- axis of ZnO [24] and correlates well with the preferred c-axis orientation of the grains seen in XRD spectra. The average diameter of the columns is largest for growth on GaAs (100) substrate, which appears to differ from the XRD results. However, it is worthwhile mentioning that XRD gives an estimation of the grain size, while the crystals observed by SEM are probably not single crystalline. The narrowest columns are observed for ZnO films on glass and Si (111) substrate. Wider, but similar, columns are observed for growth on ZnO, Si (100) and sapphire.

It is interesting to note that the trends in the microstructure (deduced from XRD) and in surface morphology (from SEM) do not track each other in terms of substrate type or orientation, nor in terms of lattice mismatch. The lattice mismatch between ZnO and the various substrates varies hugely: GaAs has the

biggest lattice mismatch with ZnO (42 %), Si (100) and Si (111) are mismatched by 40 % and 16 %, respectively, while c- and r-sapphire have atomic spacings that are 18 % and 1.6% respectively, larger than that of ZnO. One would expect grain size (and columnar width) to correlate roughly with lattice mismatch, in the sense that lower mismatch should yield a tendency for the formation of single crystalline, epitaxial films. It seems plausible that, given the rather large lattice mismatch with most substrates used here, the microstructure is not determined by mismatch, but that other factors such chemical bonding across the interface, residual oxides, substrate morphology, etc. should be taken into account.

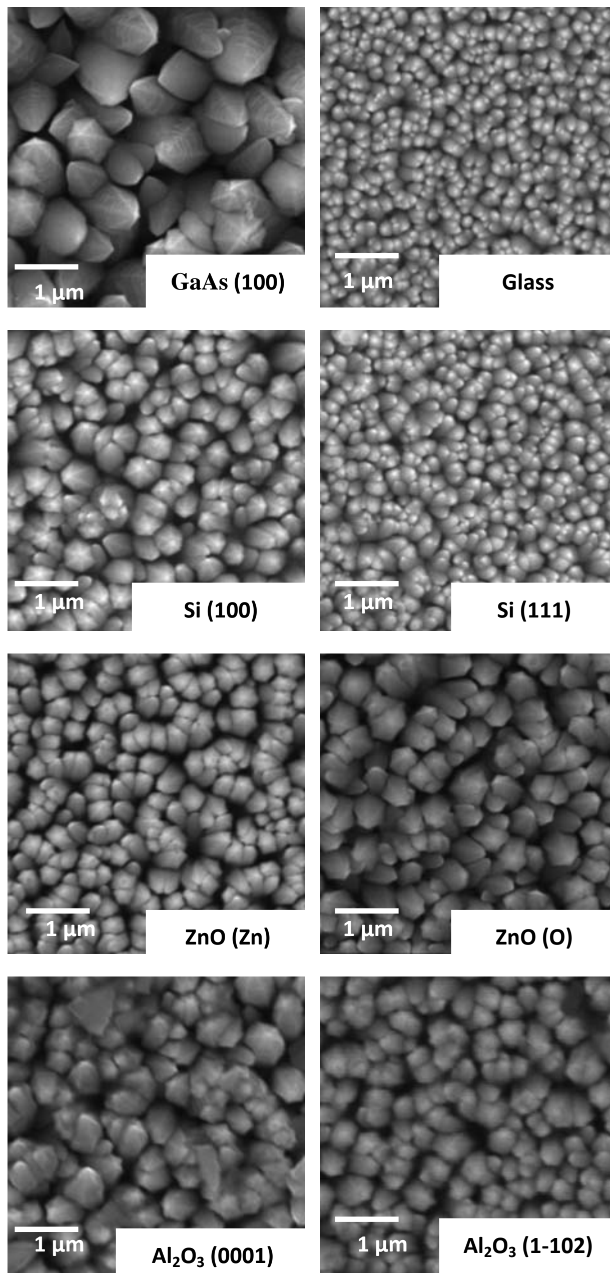

Figure 2: SEM images of a ZnO films grown on different substrates.

3.3 Photoluminescence

Fig. 4 shows the normalized low temperature PL spectra collected at 11K. The PL spectra are qualitatively similar, i.e. the same transitions are observed, but with different relative intensities. The near band-edge emission (NBE) is dominated by donor bound exciton recombination (D°X) around 3.359 eV. The free exciton (FX) appears in some of the sample at 3.374 eV which hints at a relative low defect/impurity

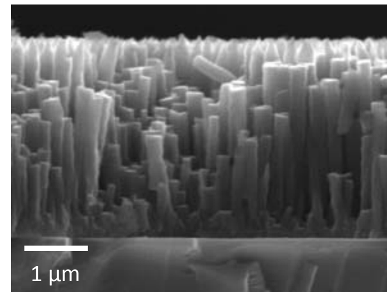

Figure 3: Cross-sectional SEM image of ZnO thin film on O-face ZnO substrate.

concentration in these samples. The insert in Fig. 4 shows a fit of the NBE of the ZnO/GaAs film. Different lines at 3.3649 eV, 3.3624 eV, 3.3596 eV and 3.3568 eV are distinguished. These have been intensively studied by many groups. Meyer *et al.* [16] assigned lines at 3.3624 eV, 3.3596 eV and 3.3568 eV to hydrogen, gallium and indium, respectively. The line at 3.3649 eV has been ascribed to Zn_i by Sann *et al.* [26]. The FWHM of the dominant line is ~2.2 meV at 11 K, compared to 1.1 meV (at 2.1 K) reported for MOCVD-ZnO by Kirchner *et al.* [27]. The small FWHM found here also indicates a relatively high quality of our layers.

The peak at 3.319 eV has been identified as free-to-bound (e, A°) transitions of electrons in the conduction band with holes localized at relatively shallow acceptor states, which are associated with basal plane stacking faults [28]. In ZnO films a high density of stacking faults are often present due to either a translation of the crystal lattice along three equivalent close-packing directions in the (0001) plane or by condensation of vacancies or interstitials to form dislocation loops accompanied by partial dislocations [28]. The peak at 3.305 eV has been ascribed to donor–acceptor pair (DAP) emission, involving the same acceptor as the (e, A^0) [28]. The higher intensity of the (e, A^0) transition for ZnO grown on glass, Si (111) and Si (100) implies a higher concentration of stacking fault-related acceptors for these substrates. It is tempting to relate the higher density of stacking faults deduced for glass and both orientations of silicon substrate to the amorphous nature of SiO_2. It seems likely that the silicon surface oxides during the annealing step (in the presence of TBOH), yielding an oxide similar in nature to glass. It is expected that nucleation and subsequent

evolution of the ZnO will be similar in these three cases. What is not understood at present is the influence of the different substrates on the lateral

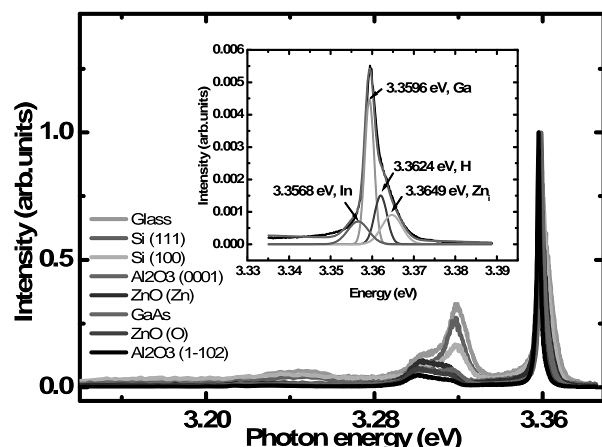

Figure 4: Normalized PL spectra at 11K for ZnO films grown on different substrate. Insert shows the fit of the NBE spectra of the ZnO/GaAs film.

dimensions of the final columnar structures. Transmission electron microscopy studies are under way to investigate the microstructure as ZnO films on the different substrates as function of thickness and substrate anneal temperature prior to growth.

3. CONCLUSION

ZnO thin films were deposited on different substrates: Si, Glass, ZnO and Al_2O_3 by metaloraganic chemical vapor deposition and the structural, morphological and optical properties have been studied. All the substrates yielded a strong degree of c-axis orientation, with grain sizes (deduced from XRD) being largest for ZnO, sapphire and Si (100) substrate. The surface morphologies were qualitatively similar, with GaAs yielding the largest hexagonal columns (up to 1 µm in diameter). The low temperature PL spectra were also qualitatively similar, although it could be deduced that growth on glass and silicon (both (100) and (111)) yielded higher stacking fault densities in the ZnO films.

4. ACKNOWLEGDGEMENT

This work is based upon research supported by the South African Research Chairs Initiative of the Department of Science and Technology and the SA National Research Foundation. The work is also supported through an AMTS grant and by the NMMU.

5. REFERENCES

[1] B. S. Li, Y. C. Liu, Z. ZZ. Zhi, D. Shen, Y. M. Lu, J. Y. Zhang, X. G. Kong, X. W. Fan: “Effect of the growth temperature on ZnO thin films grown by plasma enhanced chemical vapor deposition” *Thin Solid Films*, Vol. 414 No. 2, pp 170, 2002.

[2]D. C. Look: “Quantitative analysis of surface donors in ZnO” *Surface Science*, Vol. 601 No. 23, pp 5315-5319, 2007.

[3] H. Mitra, A. P. Chatterjee, H. S. Maiti: “ZnO thin film sensor” *Material Letters*, Vol. 35 No. 1-2, pp 33-38, 1998.

[4] Hwang D-K, Bang K-H, Jeong M-C and Myong J-M: “Effects of RF power variation on properties of ZnO thin films and electrical properties of p–n homojunction″ *Journal of Crystal Growth,* Vol. 254, pp. 449, 2003.

[5] K. Iwata, P. Fons, S. Niki, A. Yamada, K. Matsubara, K. Nakahara, T. Tanabe, H. Takasu: “ZnO growth on Si by radical source MBE” *Journal of Crystal Growth*, Vol. 214/215, pp. 50, 2000.

[6] Ziyu zhang, Yang Zhang, Li Duan, Bixia Lin, Zhuxi Fu: “Deep ultraviolet emission of ZnO films prepared by RF magnetron sputtering at changing substrate temperature” *Journal of Crystal Growth*, Vol. 290, No. 2, pp 341-344, 2006.

[7] Jie Zhao, Lizhong Hu, Zhaoyang Wang, Zhijun Wang, Heqiu Zhang, Yu zhao, Xiuping Liang: “Epitaxial growth of ZnO thin films on Si substrates by PLD technique” *Journal of Crystal Growth*, Vol. 280, No. 3-4, pp 455-461, 2005.

[8] A. Ghosh and S. Basu : “Spray/ cvd deposition and characterization of surface modified zinc oxide thickfilms for gas sensor” *Materials Chemical Physic*, Vol 27, pp 45-54, 1991.

[9] J. H. Lee, K. H. Ko, B. O. Park: “Electrical and optical properties of ZnO transparent conducting films by the sol–gel method” *Journal of Crystal Growth*, Vol. 247, No. 1-2, pp. 119-125, 2003.

[10] Jie Ren: “Initial growth mechanism of atomic layer deposition of ZnO on the hydroxylated Si(1 0 0)-2×1: A density functional theory study” *Applied Surface Science*, Vol. 255, No. 11, pp 5742, 2009.

[11] KT Roro, JK Dangbegnon, S Sivaraya, AWR Leitch, J.R. Botha: “Influence of metal organic chemical vapor deposition growth parameters on the luminescent properties of ZnO thin films deposited on glass substrates” *Journal of Applied Physics*, Vol. 103, pp 53516, 2008.[12] Jiangnan Dai, Hongbo Su, Li Wang, Yong Pu, Wenqing Fang, Fengyi Jiang: “Properties of ZnO films grown on (0 0 0 1) sapphire substrate using H2O and N2O as O precursors by atmospheric pressure MOCVD” *Journal of Crystal Growth*, Vol. 290, No. 1, pp 426-430, 2006.

[13] A.l-Yadouni, A. Boudrioua, J. C. Loulergue, Vincent Sallet, R. Triboulet : ″Growth and optical characterization of ZnO thin films deposited on

sapphire substrate by MOCVD technique" *Optical Materials*, Vol. 27, No. 8, pp 1391-1395, 2005.

[14] Zhuxi Fu, Bixai Lin, Jie Zu: "Photoluminescence and structure of ZnO films deposited on Si substrates by metal-organic chemical vapor deposition" *Thin Solid Films,* Vol. 402, No. 1, pp. 302-306, 2002.

[15] Kuy-hyun Bang, Deuk-Kyu Hwang, Sang-Wook Lim, Jae-Min Myong: "Formation of p-type ZnO film on InP substrate by phosphor doping" *Journal of Crystal Growth*, Vol. 210, No.3-4, pp. 177-182, 2003.

[16] B. K. Meyer, H. Alves, D. M. Hofmann, W. Kriegseis, D. Forster, F. Bertram, J. Christen, A. Hoffmann, M. Straßburg, M. Dworzak, U. Haboeck, and A. V. Rodina: "Bound exciton and donor-acceptor pair recombinations in ZnO" Material Sciences and Engeneering B, Vol. 127, pp. 280-284, 2006.

[17] Hongxi Liu, Hong Qiu, Xiaobai Chen, Mingpeng Yu , Mingwen Wang: "Structural and physical properties of ZnO:Al films grown on glass by direct current magnetron sputtering with the oblique target" *Current Applied Physics*, Vol. 9 pp. 1217–1222, 2009 .

[18] X. Jiang, C. L. Jia, R. J. Hong: "Microstructure dependence of ZnO: Al films on the deposition conditions and the surface morphology of silicon substrate" *Journal of Crystal growth*, Vol. 289, No. 2, pp. 464 - 471, 2006.

[19] C. Munuera, J. Zuniga-Perez, J.F. Rommeluere, V. Sallet, R. Triboulet, F. Soria, V. Munoz-Sanjose, C. Ocal : "Morphology of ZnO grown by MOCVD on sapphire substrates" *Journal of Crystal Growth,* Vol. 264, pp. 70–78, 2004.

[20] S. Agouram, J. Zuniga-Perez, V. Munoz-sanjose : "Structural and morphological characterizations of ZnO films grown on GaAs substrates by MOCVD" *Applied Physics A*, Vol. 88, pp. 83–87 2007.

[21] 94W. Göpel, J. Pollmann, I. Ivanov, and B. Reihl: ""*Physical Review B*, Vol. 26, pp. 3144, 1982.

[22] Yinzhen Wang, Shunquan Wang , Shengming Zhou , Jun Xu, Jiandong Y, Shulin Gu, Rong Zhang, Qiushi Ren: "Effects of sapphire substrate annealing on ZnO epitaxial films grown by MOCVD" *Applied Surface Science*, Vol. 253, pp. 1745–1747, 2006

[23] K. Black, A. C. Jones, P. R. Chalker, J. m. Gaskell, R. T. Murray, T. B. Joyce, s. A. Rushworth: "MOCVD of ZnO thin films for potential use as compliant layers for GaN on Si" *Journal of Crystal Growth*, Vol. 310, pp. 1010-1014, 2008.

[24] A. Van Drift: "Evolutionary selection, a principle governing growth orientation in vapour-deposited layers" Philips *Research Reports*, Vol. 22, pp. 267, 1967.

[25] J. Sann, J. Stehr, A. Hofstaetter, and D. M. Hofmann, U. Haboeck, A. Hoffmann, and C. Thomsen : "Zn interstitial related donors in ammonia-treated ZnO powders" Physical review, Vol. 76, pp 195203, 2005

[26] C. Kirchner, Th. Gruber, F. Reuss, K. Thonke, A. Waag, Ch. Geissen, M. heuken: "MOVPE growth of ZnO using various oxygen precursors" *Journal of Crystal Growth*, vol. 248, pp. 20, 2003

[27] M. Schirra, R. Schneider, A. Reiser, G. M. Prinz, M. Feneberg, J. Biskupek, U. Kaiser, C. E. Krill, K. Thonke, and R. Sauer: "Stacking fault related 3.31-eV luminescence at 130-meV acceptors in zinc oxide" Physical Review B, vol.77, Issue 12.

3D ULTRA-FAST MANUFACTURED MICRO COILS ON POLYMER OR METAL CORES

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Abstract: We present high aspect ratio 3D solenoidal micro coils manufactured in a serial, high speed and fully MEMS compatible winding procedure using an automatic wire bonder. The coils are wound on steel, glass, or polymer cores with a diameter ranging from 100 µm to 1 mm. The applications of these coils are manifold: as semi-integrated inductors for electronics, for energy harvesting purposes, and for sensors and actuators.

Key words: micro coil, manufacturing, wire bonder, SU-8.

1. INTRODUCTION

The development of 3D high aspect ratio micro solenoids and Helmholtz micro coils proved to be a challenging task for the MEMS community mainly because the traditional microfabrication techniques inherently generate 2D structures. Many groups have focused their research efforts towards obtaining 3D micro coils in the past decade. Peck et al. [1] and Seeber et al. [2] have used a hand-winding technique to produce micro coils by wrapping a wire around a capillary. This procedure is not compatible with batch-fabrication since each coil must be treated individually, with consequences on the yield and reproducibility of the manufactured coils. An interesting but rather complicated technique reported by Rogers et al. [3] involved micro-contact printing combined with a rolling process and subsequent electroplating to define coils around a capillary tube. An innovative approach by Dohi et al. [4] combines surface micromachining and a post-release folding process to create freestanding micro coils. Ehrmann et al. recently reported [5] a MEMS-compatible technology to create micro solenoids and Helmholtz micro coils using three electroplated copper layers and vias through SU-8 isolation layers. While this is a batch-fabrication technique, due to the planar nature of the processes involved, the aspect ratio of the coils, therefore their 3D character is rather limited.

We have has recently reported [6] a method to fabricate coils with sub-millimeter dimensions on PCB substrates exploiting the unique capabilities of an automatic wire bonder. However, this is not compatible with wafer-scale fabrication, therefore unsuitable for MEMS applications.
Here, we report a fully MEMS-integrated process for micro coil fabrication using the automatic wire bonder in conjunction with traditional microfabrication techniques: CrAu evaporation on Si or Pyrex substrate together with UV photolithography is used to define the metal pads for coil winding. Cylindrical posts to support the micro coils are defined using thick SU-8 photolithography. Although the wire-bonder based technique to manufacture the micro coils is a serial technique, it is compatible with the previously mentioned standard batch-fabrication techniques due to the fact that it is very fast and reproducible.
In addition to this cleanroom process, we introduce a PCB based technology as a substrate for the coils. In the following these two aspects are described in more detail.

2. MICRO COIL WINDING

Modern automatic wire bonders allow the user to define 3D coordinates, to which the bondhead moves consecutively. Our method for solenoidal coils is the following: we locate the first contact ("ball") next to a core and move circularly around the core whereas the wire plastically deforms to the core's shape. The trajectory then is terminated with the second ("wedge") bond. A schematic of the used trajectory is shown in Figure 1.
The method eliminates the loose wire end issue of other winding methods, and hence the need for manual re-soldering of the micro coils.

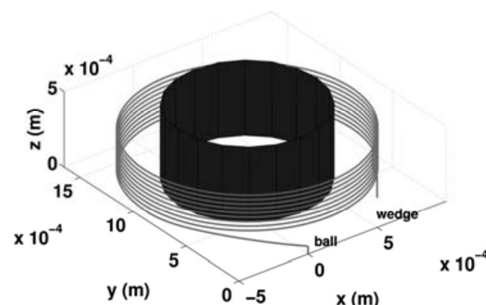


Figure 1: Wire bond trajectory.

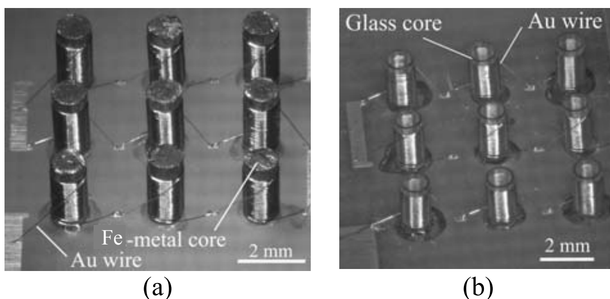
We are thus able to wind large arrays of 3D micro coils in an easy and reproducible process with an accuracy of better than 3 µm, taking 200 ms to wind a single coil. We use insulated gold wire (X-Wire™ from Microbonds) with a diameter of 25 µm.
Figure 2 is a microscope photograph taken during the coil winding process.

Figure 2: Capture of the wire bonder head in movement during the micro coil winding process.

3. SUBSTRATE PROCESSING

In this paper we present two possible substrates for micro coils: a printed circuit board (PCB) with metal or glass cores, and a fully MEMS compatible process with Pyrex or silicon wafers and SU-8 cores.

The first approach is based on PCB technology: A 1 mm thick PCB with the necessary holes and gold pads was commercially fabricated [7]. Coil cores with a total length of 3 mm were glued into the holes in the PCB, so the length of the cores above the PCB is 2 mm. Two different coil core materials were used: iron cores and hollow glass cores. Iron cores were manufactured by EDM (electrical discharge machining) erosion. The glass cores were sawed. The diameter of both cores was 1.0 mm. In Figure 3 photos of a coil array with iron cores and glass cores, respectively, is shown. The non-insulted gold bond wire is 28 µm thick. In order to avoid short-circuits a pitch of 25 µm was introduced separating the windings form each other. The number of windings is thus mainly defined by the wire diameter, the pitch, and the height if the posts.

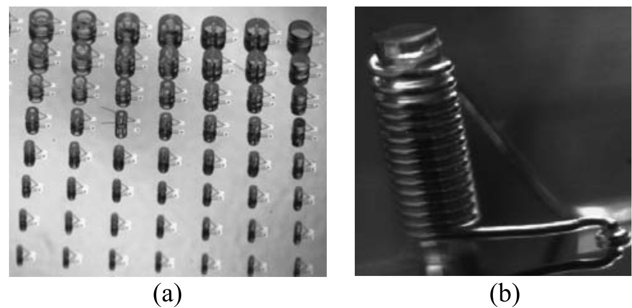


(a) (b)

Figure 3: PCB board with an array of coils around Fe-metal cores (a) and hollow glass cylinders (b).

In the second approach we first have to define the metal pads for the connection of the wire ends of the micro coils: a chromium/gold layer of 50/500 nm thickness was evaporated on the substrate. AZ 1518 photoresist was UV patterned and the chromium/gold metal was subsequently wet-etched to define the pads.

For polymer cores a thick photoresist, SU-8, was deposited onto the substrate and lithographically structured with high aspect ratio. We were able to fabricate structures with a diameter down to 100 µm and a height of up to 650 µm, resulting in an aspect ratio of 6.5:1.
In figure 4(a) a large array of micro coils wound around SU-8 posts with diameters from 1000 µm (upper line) to 200 µm (bottom line) is pictured. Figure 4(b) shows a side view of a micro coil with 150 µm diameter and 15 windings. The SU-8 post is 650 µm high. Here, we used insulted wire of 25 µm thickness.



(a) (b)

Figure 4: Micro coils around SU-8 cores.

Figure 5 shows an overview of the process steps of the wire bonded coils around SU-8 structures.

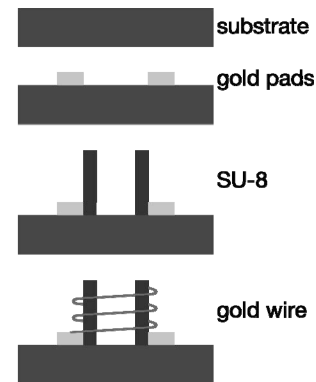
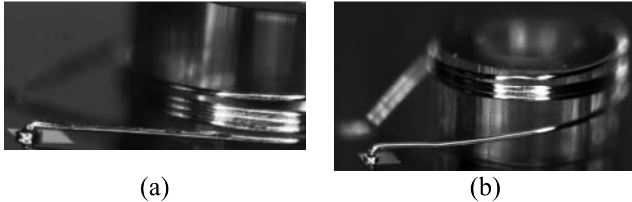


Figure 5: Process flow.

4. MEASUREMENT RESULTS

With the micrometer positioning precision of the wire bonder head, we have good control over each axis. In particular, the *z*-axis movement can be used to start the coil winding process at different heights. Figure 6 shows coils produced with different *z*-start heights. In figure 6(a) the starting height was 50 µm, what is the minimal *z*-start height. In figure 6(b) the start is 350 µm.
The pictures show that the angle of the wire between the ball and winding is almost 90° in both cases. In the case of larger starting heights, the first winding is needed to reach the desired height. Afterwards the coil is wound regularly.



(a) (b)

Figure 6: Coils with different *z*-start heights.

For electrical characterization of the coils we used an Agilent E4991A impedance analyzer. The measured real and imaginary part of the complex impedance Z corres-pond to the resistance R = real(Z) and the inductance L = imag(Z)/ω of a straight forward R-L series inductor model, where ω is the angular frequency. The quality factor Q of a coil described by this model is given by Q = imag(Z)/real(Z).

In Figure 7 the measured data for an example coil with a diameter of 100 µm, 5 windings, and a pitch of 50 µm manufactured on a glass substrate is shown. The inductance is constant at 41 nH in this frequency range. The resistance increases due to skin and proximity effects. The quality factor at 400 MHz is 41.

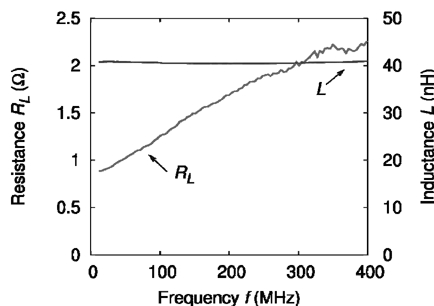


Figure 7: Frequency dependent resistance and inductance of a coil with a diameter of 100 µm, 5 windings, and a pitch of 50 µm, manufactured on a glass substrate.

5. CONCLUSION

We have manufactured coils on iron, polymer, and glass cores. Iron and glass cores were up to 2 mm high with a diameter of 1 mm, polymer cores up to 650 µm tall with a minimal diameter of 100 µm. These small cores carry up to 15 windings of 25 µm diameter gold wire.

The introduced production method for micro coils is not only compatible with standard micro manufacturing processes, we also believe that it is competitive with SMD technology. The possibility of adapting the inductance by the free choice of the number of windings as well as the relatively free choice of the core diameter, combined with the fact that no subsequent soldering is required, offer a flexibility and a semi-integration level which provides a tremendous advantage for micro-electronics, RF technology, measurement technique, and sensors.

6. ACKNOWLEDGMENTS

The authors acknowledge project funding by the EU NEST Project number 028533. We thank the IMTEK clean room staff for supporting us with the wafer preparation. We gratefully acknowledge technical support from *ESEC Ltd*.

7. REFERENCES

[1] T.L. Peck, R.L. Magin, and P.C. Lauterbur: "Design and Analysis of Microcoils for NMR Microscopy", *Journal of Magnetic Resonance*, vol. 108, pp. 114-124, 1995.

[2] D.A. Seeber, R.L. Cooper, L. Ciobanu, and C. H. Penningtona: "Design and Testing of High Sensitivity Microreceiver Coil Apparatus for Nuclear Magnetic Resonance and Imaging", *Review of Scientific Instruments*, vol. 72, no. 4, pp. 2171–2179, 2000.

[3] J.A. Rogers, R.J. Jackman, and G.M. Whitesides: "Using Microcontact Printing to Fabricate Microcoils on Capillaries for High Resolution Proton NMR on Nanoliter Volumes", *Appl. Phys. Lett.*, vol. 70, no. 18, pp. 2464–2466, 1997.

[4] T. Dohi, K. Kuwana, K. Matsumoto, and I. Shimoyama: "A Standing Micro-coil for a High Resolution MRI", *Proc. of Transducers 2007*, pp. 1313-1315.

[5] K. Ehrmann, N. Saillen, F. Vincent, M. Stettler, M. Jordan, F.M. Wurm, P.-A. Besse, and R. Popovic: "Microfabricated Solenoids and Helmholtz Coils for NMR Spectroscopy of Mammalian Cells", *Lab on a Chip*, vol. 7, pp. 373-380, 2007.

[6] K. Kratt, M. Seidel, M. Emmenger, U. Wallrabe, and J.G. Korvink: "Solenoidal micro coils manufactured with a wire bonder", *Proc. of IEEE MEMS 2008*, pp. 996-999.

[7] http://www.contag.de, Webpage accessed on August 11, 2008.