# SILICON$^+$ - POST PROCESSING CMOS WAFERS TO CREATE INTEGRATED SENSORS, MEMS AND ELECTRO-OPTIC SYSTEMS

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**Abstract:** Silicon based integrated circuit technology has shown astonishing progress scaling to smaller geometries as the industry follows Moore's predictions. However, in recent years the cost associated with staying at the leading edge of silicon IC technology has resulted in many companies being either unable, or unwilling, to afford the investment required. As a consequence some have decided to use foundry technology and/or diversify into new device types and associated novel application areas. All of these diverse Silicon$^+$ technologies have one particular feature in common, namely they all use silicon as a platform for system integration with the added value being the innovation associated with post-processing and/or technology integration, which in many cases is realised on standard foundry technology. This paper examines many of the issues associated with integrating foundry and custom IC wafers with both new materials and technologies such as MEMS based sensors and actuators. In particular it examines the various options available for companies considering Silicon$^+$ technology applications and presents examples of successful applications of this approach. Some of these are illustrated below.

**Key words:** silicon post processing CMOS integrated sensors, MEMS, electro-optic systems

## 1. INTRODUCTION

As the costs of following the International Technology Roadmap for Semiconductors (ITRS) [1] increase, a higher percentage of IC manufacturing companies are unable to afford the capital investment required to competitively manufacture the next technology node. To help reduce the risks most companies who are still committed to the next node in the roadmap, have joined forces with others to form consortia to reduce R&D costs by sharing the burden. Even with sharing the cost of developing technologies for the next generation of CMOS technology there is still a significant number of firms that are unable to sustain the investment required to follow Moore's law. These companies clearly have a technology resource they wish to exploit and are increasingly seeking to follow a more diversified business model to protect revenues. Hence, there is an interest in targeting products with additional functionalities deriving from biological, chemical, mechanical, optical, and other domains, to develop enhanced products and move into building systems rather than components. In following this strategy new and larger markets are created for these products, which have been traditionally outside the typical electronics-based portfolio of IC based companies. Some examples of these emerging technologies are detailed in the ITRS Roadmap and are listed below

- MEMS / Microsystems
- Photonics
- Plastics Electronics

The above technologies have one particular feature in common, namely they can they can be significantly enhanced by employing silicon as a platform for system integration. In this case the added value comes from the innovation associated with post-processing new/novel materials and technologies on CMOS or bipolar technology. In many cases this post-processing will be on standard foundry technologies taking full advantages of the economies of scale available as silicon microelectronics continues its remarkable evolution to smaller and smaller geometries.

Examples of this diversification that are presently being exploited includes smart power (integration of power devices with microelectronics), RF systems (integration of other semiconductor technologies such as SiGe, GaAs and passives with CMOS), microsystems (integration of a wide range of MEMS devices and sensors with CMOS), microdisplays (liquid crystal, light emitting polymers with the driving microelectronics on silicon directly underneath the display technology), bioelectronics (lab on a chip) and silicon photonics (integration of optical components on a silicon platform). All of these Silicon$^+$

technologies[*] have one element in common, namely the use of silicon as a platform for system integration with the added value being the innovation associated with post-processing and/or integration.

The attraction of silicon as a platform technology arises from its dominance as a high performance cost effective technology, which to date is unchallenged. However, it is clear that the scaling of Silicon IC technology cannot continue forever and either the economics associated with the reduction of dimensions or the limits of physics will initially slow and then halt the process. When scaling has run its course and the technology enters a more mature phase the importance of Silicon[+] as a source for innovation and new product developments will increase.
The vision of Silicon[+] in this paper is that it effectively treats the platform silicon integrated circuit (IC) technology as a commodity element of the system, and with much of mainstream CMOS being foundry based, the value added part becomes the bespoke processing and the associated IP. One of the attractions of this approach is that state-of-the-art CMOS technology is readily available without the need for any capital investment, which is a business model which has been very successfully exploited by so called fabless companies. The major appeal of this approach is that as foundry-processes are updated, the technology is immediately accessible making this element of any technology/product development future-proofed without the requirement for any significant capital investment. Hence, the potential exists for Silicon[+] based SMEs and startup companies to readily exploit new technology nodes as they become available.

This paper[•] will examine the options and challenges associated with integrating both foundry and custom IC technology with both new materials and other technologies such as MEMS (sensors and actuators) and present examples of the various options.

## 2. MEMS[‡]/CMOS[†] INTEGRATION

The performance of many sensors and Micro-Electro-Mechanical Systems (MEMS) can profit from being directly integrated with electronics. For example, there are great benefits in connecting pre-amplifiers and signal conditioning close to sensors, providing considerable advantages in performance and cost. Furthermore, if large arrays of sensors and/or actuators are required then backplane silicon electronics becomes essential.

There are a number of options available for integrating MEMS and CMOS integrated circuit technologies. The key requirements are to implement electrical, and in some cases thermal, interconnect between the CMOS and MEMS elements and some of the options that are available are listed below:

(a) The MEMS devices are fabricated on an electronic grade Silicon wafer and then encapsulated in oxide. The standard CMOS process then follows [2].
(b) Foundry wafers with the required electronics are fabricated and the MEMS is then post-processed on top [3, 4]
(c) A completely integrated CMOS and MEMS process is used [5].
(d) Manufacture of MEMS devices using etch release of structures built using material layers available and patterned as part of the CMOS process [21,22].
(e) MEMS and CMOS technologies (either in wafer or chip form) are individually fabricated and hybridised [6]
(f) Multi-chip modules
(g) Wafer bonding is used to integrate CMOS with MEMS [7,8]

The first four of these involve fabricating both the microelectronic devices and the MEMS technologies on a single wafer with the remaining ones involving integrating the technologies together after their separate fabrication. All of these approaches involve compromises and so have their individual attractions and limitations [3,4 ,8,9]. The following sections discuss the above approaches and their pros and cons.

### *2.1 MEMS processed on wafer before CMOS fabrication*

In this format MEMS devices are fabricated in recesses in silicon wafers and effectively buried in oxide or some other suitable material [2] as shown in figure 1. The wafer is then planarised and the CMOS devices fabricated in the exposed silicon next to the device. The advantage of this approach is that the process is fully integrated, but the MEMS devices will experience all the high temperature steps associated with the CMOS process flow, which may cause problems for some structures. While this method of integration appears very attractive, a real practical issue with this technology is that contamination is a potential problem for all IC fabs, which precludes the use of many MEMS materials. Hence, if a MEMS fab is to manufacture the microsystem structures and bury them in oxide or some other material ready for the CMOS fabrication step then the IC foundry must have qualified the MEMS foundry to ensure that there are will be no possibility of contamination.

Another reason why this approach has not been widely adopted may be that the cost of processing the microelectronic circuitry (and also MEMS) is fixed

[*] This approach is sometimes referred to as *More than Moore* (Scaling being More Moore) and/or *heterogeneous integration*
[•] This paper is based on a presentation give at an IET Symposium (2007) and an article in the NMI Year Book (2008).
[‡] In this paper MEMS is used in its widest sense to include all sensors and actuators.
[†] When CMOS integration with MEMS is referred to this should be considered to include other integrated circuit technologies such as bipolar, Bi-CMOS etc

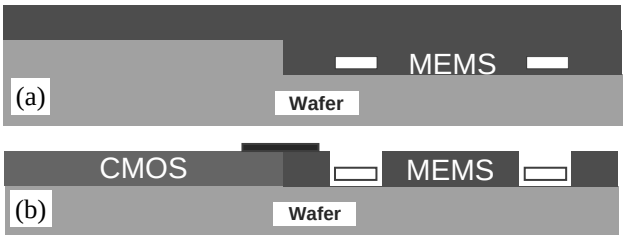


Figure 1. Schematic of MEMS processed on wafers before CMOS fabrication. (a) MEMS devices fabricated and buried in oxide which is then planarised to expose the silicon using CMP. (b) Finished process with metal interconnect between the CMOS and MEMS.

regardless of the number of devices on the wafer. Hence, the area occupied by the MEMS device can be considered to have a significant "microelectronics process" cost associated with it, especially if it is large. With the CMOS and MEMS wafer processing costs both effectively fixed, the end result is that MEMS processed on wafers before CMOS fabrication may provide significantly fewer systems than would be the case if the two technologies were fabricated on separate wafers and then assembled in a multi-chip module (see section 2.6) or as a chip on chip (see section 2.5). Obviously, where the benefits of direct integration outweigh the above considerations pre-processed MEMS will be viable but it is clear that there are significant cost penalties associated with using this approach when integrating the latest IC processes with large MEMS devices.

*2.2 Foundry wafer post-processed with MEMS*

Post-processing foundry CMOS involves procuring standard foundry processed wafers and then adding and patterning extra layers to create the MEMS device on top of the IC technology (see figure 2). The attraction of this approach is that the resulting system can select the most appropriate IC technology, and hence there is no problem procuring state-of-the-art technology should it be required. However, it should be remembered that mask sets for state-of-the-art IC technology are extremely expensive so post-processing integration with advanced processes is really only a feasible option for high volume products unless an existing design can be used as the IC backplane.

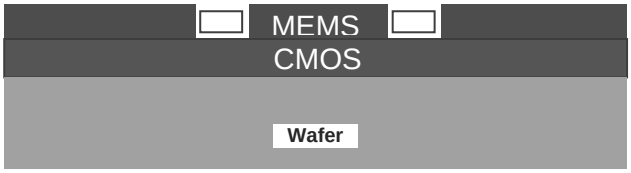


Figure 2. Schematic of foundry wafer post-processed with MEMS.

Post-processing has many attractions but one of its limitations is that the maximum processing temperature is limited to not more than 450°C to protect the integrity of the CMOS, making the use of materials such as polysilicon for resonators during the post-processing phase impractical. Possible replacements that have been proposed are germanium and SiGe [10,11] that can be deposited at 400-450°C.

There are many other standard IC (and non-standard) materials which can be deposited and patterned. Examples of companies whose commercial products follow this approach are MicroPix, (now 4D - Liquid Crystal alignment and spacer technology for LC microdisplays [12]) and Vision (before being acquired by ST Microelectronics – CMOS imagers with micromachined lenses and colour filters [13]). Another company that has successfully used this approach of post-processing foundry CMOS is Microemissive Displays (MED) with their organic light emitting diode (OLED) microdisplays [14]. Other technologies suited to this implementation include the fabrication of detectors [15] and ElectroWetting On Dielectric (EWOD) [16] devices on silicon IC backplanes. Figure 3 (a) shows an example of an EWOD chip with 25 electrodes for moving liquid droplets while figure 3 (b) shows EWOD electrodes (with a 100μm pitch) integrated with SPADs (Single Photon Avalanche Diodes). Many of the above commercialised application specific technologies that were originally post-processed have matured to the stage where they have now become part of a foundry's standard offering. Finally, it should be remembered that the post-processing option enables the final fabrication steps to be either undertaken in a custom built process line or in a contract run MEMS facility, which provides opportunities for second sourcing.

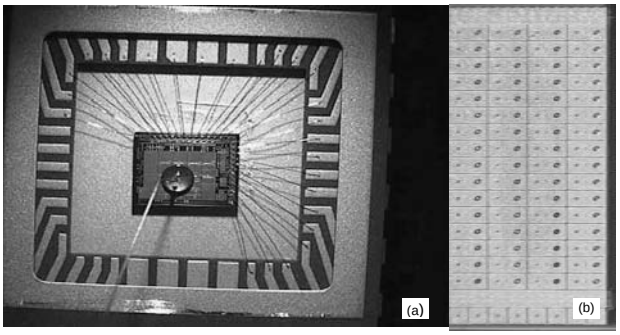


Figure 3. (a) A 25 electrode CMOS EWOD chip. (b) EWOD chip with integrated SPADs on each electrode.

*2.3 Total integration of MEMS and CMOS processes*

This option requires access to an integrated fabrication facility and is really only open to companies and organisations that are more vertically integrated having both CMOS and MEMS technology available (figure 4). The drawback of this approach is that, if there is a need to

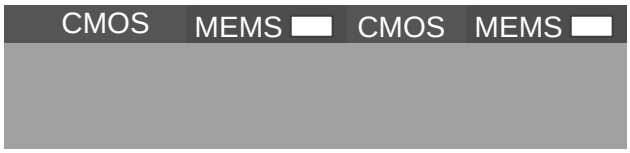


Figure 4. Schematic of the total integration of MEMS and CMOS processes.

future proof a business by keeping in-house IC technology following the roadmap, then extremely high levels of investments are required. Two examples of companies in a position to take the full integration approach, but who perhaps have not been fully committed to following the roadmap, are Texas Instruments and Analog Devices. Both have significant shares of the MEMS market with TI fabricating their Digital Micro Mirror (DMM) display system† [17] and Analog Devices their accelerometer and gyro products [18,19]. The commercial barriers to entering the market using this approach are significant as it requires a fabrication facility with both CMOS and MEMS capability, which even if the CMOS technology is not state-of-the-art, still requires significant investment. However, it does enable both the MEMS and CMOS to be optimised within the constraints of the process flow employed.

### *2.4 CMOS process with MEMS etch release/access post-process*

In this approach, the CMOS wafer is fabricated in the standard manner with the design already incorporating the layout required by the MEMS device [20]. At the completion of the CMOS process all that is required is a simple etch release step as shown schematically in figure 5. Examples of this include diffraction gratings / light filters using the multilevel fine metal pitch available with the latest processes [21], releasing mechanical structures such as comb-drive resonators, cantilever beam arrays and accelerometers [22,23], copper structures [24] and pH sensors for a pill that is swallowed (figure 6) [25,26]. Reference [3] also gives more examples of the above approach for a number of different technologies.

This method of CMOS foundry technology with MEMS etch release can obviously be used in combination with post-processing extra patterned layers either before or after the etch release step. As with standard post-processing the above approach can take full advantage of the latest IC technology with sub-micron polysilicon and metal structures being available and of course copper and low κ materials.

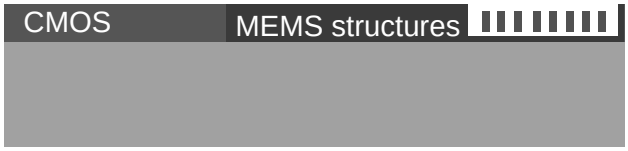


Figure 5. Schematic of a CMOS process with MEMS etch release/access post-process.

### *2.5 Hybridisation*

This scheme involves taking separately processed CMOS and MEMS wafers (or chips) and then hybridising or bump bonding them. This is a standard process that is widely used for IC packaging/interconnect and providing processing temperatures < 450°C (the maximum temperature for CMOS ICs) are used hybridisation is very straightforward (see figure 7).

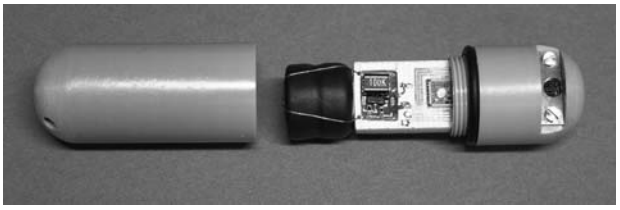

Figure 6. Sensors in a pill [25] suitable for CMOS / MEMS sensor fabricated by post CMOS etching [26].

However, for some MEMS devices the materials and or structures will not survive temperatures approaching this maximum. If low temperature bumping is required then there are a number of options that include indium [27] and gold ball bumping [28]. An example utilising indium bumps is the SCUBA-2 sub-millimetre bolometer detector [6] shown in figure 8. This 4×5cm device has 218,000 indium bump bonds providing both thermal and electrical connection between the upper pixel array and the underlying SQUID multiplex device. An example using gold bumping is the creation of micro-inductors [28], images of which are shown in figure 9. Alternatively, eutectic die bonding of CMOS - MEMS technology has been demonstrated by Austria Microsystems to produce a polysilicon based capacitive acceleration sensor bonded onto a CMOS chip containing the sensing electrode and read-out electronics [29].

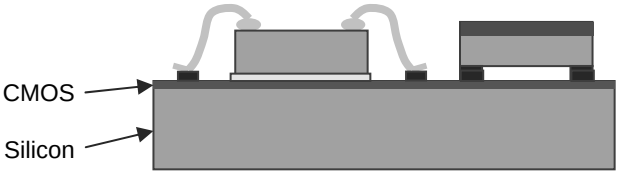


Figure 7. Flip chip and wire bonding hybridisation.

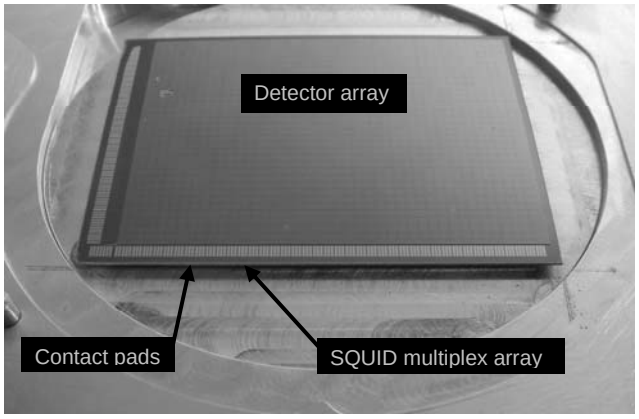


Figure 8. One quadrant of the detector array for SCUBA-2. The detector is hybridised to the bottom chip with 218,000 indium bump bonds to provide both electrical and thermal conduction.

† Note that while the DMM technology comes from a company that manufactures ICs and can be considered fully integrated the MEMS process is built on top of the electronics and so could be considered as post-processed.

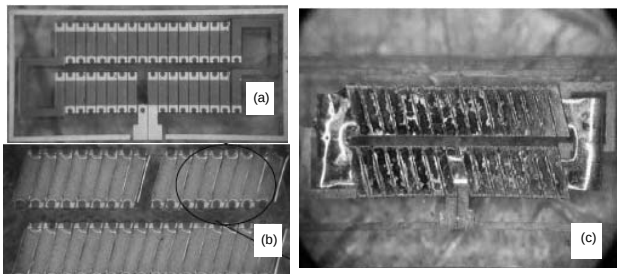


Figure 9. Fabricated micro-inductor (a) bottom, (b) top of an inductor before bump bonding, (c) micro-inductor of size 2mm×5mm×250μm (W×L×T). The nickel windings are clearly visible diagonally. The Ni(80)Fe(20) core of ring is assembled between the windings by flip-chip bonding.

It is possible to attach the MEMS device to the CMOS wafer (or *vice versa*) and subsequently provide the interconnect between chips with wire bonding (chip on chip). A further hybrid-type approach is to use what could be considered a non-MEMS technology hybridised with a CMOS backplane [30], a method used in proof of concept devices for the post-processed detector technology reported in reference [15].

*2.6 Multi-chip Modules*

Using multi-chip modules is a standard approach for assembling more than two ICs and other components, e.g. chip capacitors, into an electronic module. Being such a readily available technology this has a low entry barrier and can be used for many applications. A large number of manufacturers, including Bosch, Motorola (Freescale) and SensoNor use this approach with many of their MEMS based systems.

*2.7 Wafer bonding of CMOS and MEMS wafers*

Fabricating MEMS and CMOS devices on separate wafers enables the optimisation of each technology independently. Hence, there are many potential attractions if the two wafers can be combined together. However, bonding two wafers together, to integrate the two technologies, requires a low temperature (<450°C†) bonding step to prevent any thermal effects or damage to the processed wafers. In addition, some method of electrically connecting the bonded wafer pair and bringing the electrical signals to the top surface also needs to be implemented. The electrical interconnect issue has many solutions that are well documented in 3-D interconnect research such as [31,32]. References [7,8] present details of test structures that have been designed to examine the feasibility of integrating prefabricated MEMS and CMOS devices (see figure 10), using chemical mechanical polishing (CMP) and low temperature wafer bonding. An example of this is shown in figure 11.

† Note: This temperature can be considerably lower depending upon the materials being used

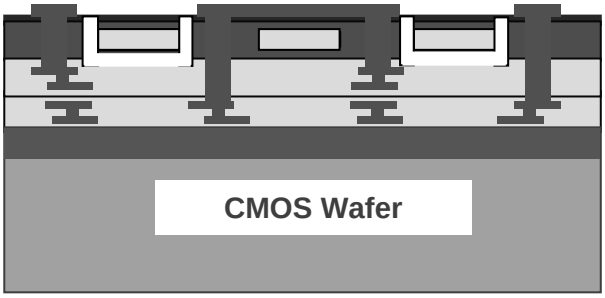


Figure 10. Schematic of integrating MEMS with CMOS using wafer bonding and thinning.

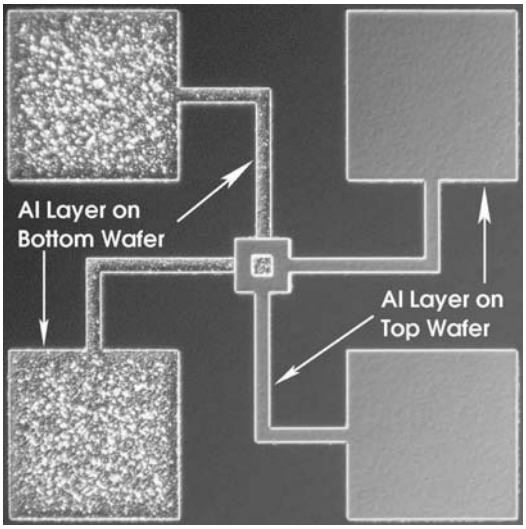


Figure 11. Bonded and electrically connected structures (via in centre of photograph). The top silicon handle wafer has been removed and the pattern on the bottom wafer can be viewed through the oxide.

Wafer bonding requires that the CMOS and MEMS die must be designed to have the same pitch on the wafer which can lead to unused areas of silicon on one of the wafers. From a commercial point of view the best ratio for the CMOS and MEMS working areas is 1:1 where there is no unused/wasted real estate for either the CMOS or MEMS technology. Figure 12 shows this effect as a

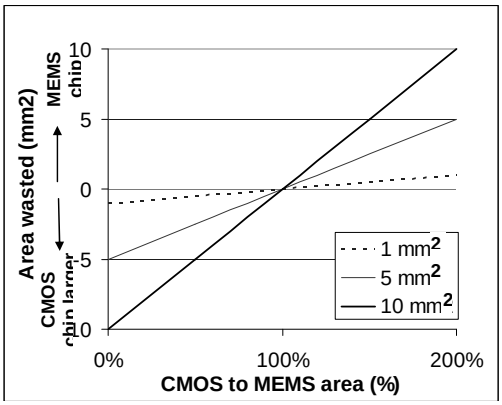


Figure 12. Relationship between MEMS and CMOS area that remains unused for bonded wafers as the ratio of the chip size of the two technologies varies. MEMS and CMOS chip sizes are 1, 2 and 10mm$^2$ when CMOS to MEMS chip area ratio = 100%.

function of chip size and ratio of CMOS to MEMS chip area. Obviously with chip based hybridisation there is not such an issue as the chips are diced before interconnect and hence there is no need for the chips to be identical sizes.

## 3. DISCUSSION AND CONCLUSIONS

The exponential increase in IC performance, which has followed Moore's Law for 40 years, has used the ITRS (International Technology Roadmap for Semiconductors) scaling rules to good effect. This has enabling the IC industry and its customers to plan their businesses effectively, as the roadmap has reliably predicted the rollout and price/performance of the next generation circuit node. With the maturing of silicon IC technology, following the roadmap has become more expensive and the number of active players has reduced. Further shrinking of the component scale is now approaching physical and economic limits, while at the same time microelectronic devices are becoming all pervasive within society and are increasingly being combined with a plethora of other sensing and processing technologies. We face a disruptive discontinuity in that:

- A large percentage of IC companies will not be able to afford to continue following the ITRS roadmap (this has already happened to almost all the UK based manufacturing operations) and the industry will increasingly have to follow a diversified business model to protect revenues.
- Beyond traditional IC electronic processing, the incorporation of additional functionalities deriving from biological, chemical, mechanical, optical or other domains will increasingly be targeted by IC companies to develop enhanced silicon technology, creating new and larger markets beyond the existing electronics-based openings.

This presents CMOS and MEMS technology with new methods of enabling continued growth in the performance of IC technology through the innovative implementation and integration of MEMS, novel materials and technology with silicon ICs.

Exploiting the technological opportunities at the interface between silicon electronics, engineering and the physical and life sciences is obviously crucial to the objective of following the opportunities presented by Silicon$^{+}$. Developments in this area will, for example, see a transformation in devices such as bioarrays, sensors and medical diagnostics, which integrate state of the art semiconductor technology with surface chemistry and biochemistry and which necessitate interdisciplinary collaboration. In parallel, there is the potential to harness existing technologies and integrate them with new materials and other circuitry. Therefore, with appropriately multi-skilled teams it will be possible to harness the power of photonics, microfluidics, chemical sensing and micro-mechanical functions with the processing power of electronics. This in turn will help create new and exciting opportunities for both research and industry centred on the effective implementation of MEMS related technology using silicon as a high-performance versatile platform technology.

| Process | Cost barrier to entry | Wafer scale | Pre-tested dies | Commercial availability | Die assembly | High temp MEMS |
|---|---|---|---|---|---|---|
| Pre-CMOS MEMS Integrated | Medium/ High | Yes | No | Limited | No | Yes |
| Post-processed MEMS on CMOS | Medium | Yes | No | Some processes | No | No |
| Integrated CMOS and MEMS | High | Yes | No | Extremely limited | No | Possible |
| CMOS and MEMS with etch release | Medium/Low | Yes | No | Yes | No | Possible |
| Hybridisation | Low | Yes | Yes - die/die No - waferscale | Yes (die) | Yes | Yes |
| Chip on chip | Low | No | Yes | Yes | Yes | Yes |
| Multi-chip Module | Low | No | Yes | Yes | Yes | Yes |
| CMOS/MEMS wafer bonding | Medium | Yes | No | No | No | Yes |

Table 1. Comparison of different CMOS / MEMS integration technologies.

The method of integration selected will be entirely driven by cost and table 1 compares some aspects of the different options. One issue for all the options is the availability of second sourcing which is usually required and this may be more problematic for the fully integrated approach, although large vertically integrated companies usually have more than one manufacturing site.

The post-processing option has many attractions to start-up companies as has been illustrated by companies such as MED, MicroPix and Vision (ST), who have successfully developed microdisplays and CMOS imagers. While it is clear that some options are only available to large IC companies, the post-processing option can clearly be successfully exploited by a wider range of organisations as can the hybridisation related approaches. Both of these approaches have a lower cost of entry and so have attractions.

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